ANALOG DEVICES

Quad, 8-Bit, 100 MSPS Serial LVDS 1.8 V A/D Converter

AD9287

FEATURES

Four ADCs integrated into 1 package
133 mW ADC power per channel at 100 MSPS
SNR = 49 dB (to Nyquist)
ENOB = 7.85 bits
SFDR = 65 dBc (to Nyquist)
Excellent linearity
- **DNL = ±0.2 LSB (typical)**
- **INL = ±0.2 LSB (typical)**

Serial LVDS (ANSI-644, default)
- **Low power reduced signal option, IEEE 1596.3 similar**

Data and frame clock outputs
295 MHz full power analog bandwidth
2 V p-p input voltage range
1.8 V supply operation
Serial port control
- **Full-chip and individual-channel power-down modes**
- **Flexible bit orientation**
- **Built-in and custom digital test pattern generation**
- **Programmable clock and data alignment**
- **Programmable output resolution**
- **Standby mode**

APPLICATIONS

Medical imaging and nondestructive ultrasound
Portable ultrasound and digital beam forming systems
Quadrature radio receivers
Diversity radio receivers
Tape drives
Optical networking
Test equipment

GENERAL DESCRIPTION

The AD9287 is a quad, 8-bit, 100 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit that is designed for low cost, low power, small size, and ease of use. The product operates at a conversion rate of up to 100 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock (DCO) for capturing data on the output and a frame clock (FCO) for signaling a new output byte are provided. Individual channel power-down is supported and typically consumes less than 2 mW when all channels are disabled.

FUNCTIONAL BLOCK DIAGRAM

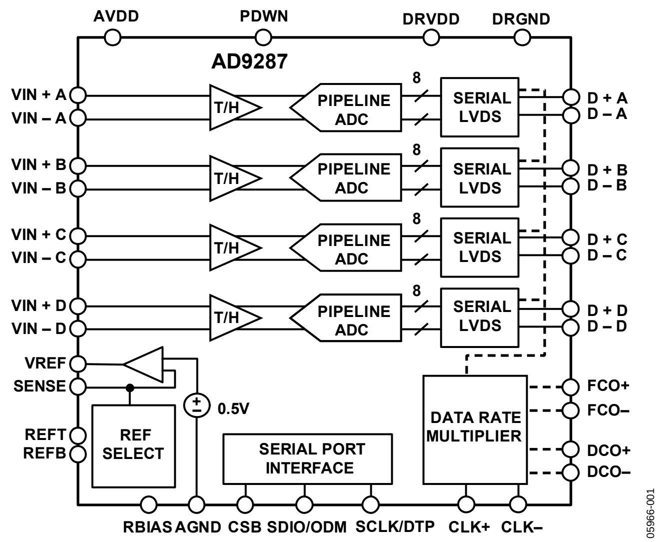


Figure 1.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI®).

The AD9287 is available in a Pb-free, 48-lead LFCSP package. It is specified over the industrial temperature range of –40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Small Footprint. Four ADCs are contained in a small, space-saving package; low power of 133 mW/channel at 100 MSPS.
2. Ease of Use. A data clock output (DCO) is provided that operates up to 400 MHz and supports double data rate operation (DDR).
3. User Flexibility. Serial port interface (SPI) control offers a wide range of flexible features to meet specific system requirements.
4. Pin-Compatible Family. This includes the AD9219 (10-bit), AD9228 (12-bit), and AD9259 (14-bit).

Rev. 0

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REVISION HISTORY

7/06—Revision 0: Initial Version

SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −0.5 dBFS, unless otherwise noted.

Table 1.

		AD9287-100			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		8			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full		±5	±23.4	mV
Offset Matching	Full		±5	±23.4	mV
Gain Error	Full		±6		% FS
Gain Matching	Full		±0.5	±2	% FS
Differential Nonlinearity (DNL)	Full		±0.2	±0.8	LSB
Integral Nonlinearity (INL)	Full		±0.2	±0.65	LSB
TEMPERATURE DRIFT					
Offset Error	Full		±2		ppm/°C
Gain Error	Full		±17		ppm/°C
Reference Voltage (1 V Mode)	Full		±21		ppm/°C
REFERENCE					
Output Voltage Error (VREF = 1 V)	Full		±5	±30	mV
Load Regulation @ 1.0 mA (VREF = 1 V)	Full		3		mV
Input Resistance	Full		6		kΩ
ANALOG INPUTS					
Differential Input Voltage Range (VREF = 1 V)	Full		2		V p-p
Common-Mode Voltage	Full		AVDD/2		V
Differential Input Capacitance	Full		7		pF
Analog Bandwidth, Full Power	Full		295		MHz
POWER SUPPLY					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
IAVDD	Full		260	274	mA
IDRVDD	Full		34.5	38	mA
Total Power Dissipation (Including Output Drivers)	Full		530	562	mW
Power-Down Dissipation	Full		2	4	mW
Standby Dissipation[2]	Full		72		mW
CROSSTALK	Full		−100		dB
CROSSTALK (Overrange Condition)[3]	Full		−100		dB

[1] See the AN-835 Application Note, "Understanding High Speed ADC Testing and Evaluation," for a complete set of definitions and how these tests were completed.
[2] Can be controlled via SPI.
[3] Overrange condition is specific with 6 dB of the full-scale input range.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −0.5 dBFS, unless otherwise noted.

Table 2.

Parameter[1]		Temp	AD9287-100 Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)	f_{IN} = 2.4 MHz	Full		49.2		dB
	f_{IN} = 49.7 MHz	Full	46.5	49.0		dB
	f_{IN} = 70 MHz	Full		49.0		dB
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)	f_{IN} = 2.4 MHz	Full		49.0		dB
	f_{IN} = 49.7 MHz	Full	46.0	48.5		dB
	f_{IN} = 70 MHz	Full		48.5		dB
EFFECTIVE NUMBER OF BITS (ENOB)	f_{IN} = 2.4 MHz	Full		7.88		Bits
	f_{IN} = 49.7 MHz	Full	7.43	7.85		Bits
	f_{IN} = 70 MHz	Full		7.85		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)	f_{IN} = 2.4 MHz	Full		70.0		dBc
	f_{IN} = 49.7 MHz	Full	54.0	65.0		dBc
	f_{IN} = 70 MHz	Full		62.0		dBc
WORST HARMONIC (Second or Third)	f_{IN} = 2.4 MHz	Full		−70.0		dBc
	f_{IN} = 49.7 MHz	Full		−65.0	−54.0	dBc
	f_{IN} = 70 MHz	Full		−62.0		dBc
WORST OTHER (Excluding Second or Third)	f_{IN} = 2.4 MHz	Full		−77.0		dBc
	f_{IN} = 49.7 MHz	Full		−74.0	−58.5	dBc
	f_{IN} = 70 MHz	Full		−71.0		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = −7.0 dBFS	f_{IN1} = 15 MHz, f_{IN2} = 16 MHz	25°C		70.0		dBc
	f_{IN1} = 70 MHz, f_{IN2} = 71 MHz	25°C		68.5		dBc

[1] See the AN-835 Application Note, “Understanding High Speed ADC Testing and Evaluation,” for a complete set of definitions and how these tests were completed.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −0.5 dBFS, unless otherwise noted.

Table 3.

Parameter[1]	Temp	AD9287-100 Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	250			mV p-p
Input Common-Mode Voltage	Full		1.2		V
Input Resistance (Differential)	25°C		20		kΩ
Input Capacitance	25°C		1.5		pF
LOGIC INPUTS (PDWN, SCLK/DTP)					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC INPUT (CSB)					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		70		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC INPUT (SDIO/ODM)					
Logic 1 Voltage	Full	1.2		DRVDD + 0.3	V
Logic 0 Voltage	Full	0		0.3	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
LOGIC OUTPUT (SDIO/ODM)					
Logic 1 Voltage (I_{OH} = 50 μA)	Full	1.79			V
Logic 0 Voltage (I_{OL} = 50 μA)	Full			0.05	V
DIGITAL OUTPUTS (D+, D−), (ANSI-644)[1]					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	247		454	mV
Output Offset Voltage (V_{OS})	Full	1.125		1.375	V
Output Coding (Default)			Offset binary		
DIGITAL OUTPUTS (D+, D−), (Low Power, Reduced Signal Option)[1]					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	150		250	mV
Output Offset Voltage (V_{OS})	Full	1.10		1.30	V
Output Coding (Default)			Offset binary		

[1] See the AN-835 Application Note, "Understanding High Speed ADC Testing and Evaluation," for a complete set of definitions and how these tests were completed.
[2] This is specified for LVDS and LVPECL only.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −0.5 dBFS, unless otherwise noted.

Table 4.

Parameter[1]	Temp	AD9287-100 Min	Typ	Max	Unit
CLOCK[2]					
Maximum Clock Rate	Full	100			MSPS
Minimum Clock Rate	Full			10	MSPS
Clock Pulse Width High (t_{EH})	Full		5		ns
Clock Pulse Width Low (t_{EL})	Full		5		ns
OUTPUT PARAMETERS[2]					
Propagation Delay (t_{PD})	Full	2.0	2.7	3.5	ns
Rise Time (t_R) (20% to 80%)	Full		300		ps
Fall Time (t_F) (20% to 80%)	Full		300		ps
FCO Propagation Delay (t_{FCO})	Full	2.0	2.7	3.5	ns
DCO Propagation Delay (t_{CPD})[3]	Full		t_{FCO} + (t_{SAMPLE}/16)		ns
DCO to Data Delay (t_{DATA})[3]	Full	(t_{SAMPLE}/16) − 300	(t_{SAMPLE}/16)	(t_{SAMPLE}/16) + 300	ps
DCO to FCO Delay (t_{FRAME})[3]	Full	(t_{SAMPLE}/16) − 300	(t_{SAMPLE}/16)	(t_{SAMPLE}/16) + 300	ps
Data to Data Skew ($t_{DATA-MAX}$ − $t_{DATA-MIN}$)	Full		±50	±150	ps
Wake-Up Time (Standby)	25°C		600		ns
Wake-Up Time (Power Down)	25°C		375		µs
Pipeline Latency	Full		10		CLK cycles
APERTURE					
Aperture Delay (t_A)	25°C		500		ps
Aperture Uncertainty (Jitter)	25°C		<1		ps rms
Out-of-Range Recovery Time	25°C		2		CLK cycles

[1] See the AN-835 Application Note, "Understanding High Speed ADC Testing and Evaluation," for a complete set of definitions and how these tests were completed.
[2] Can be adjusted via the SPI interface.
[3] t_{SAMPLE}/16 is based on the number of bits multiplied by 2; delays are based on half duty cycles.

TIMING DIAGRAMS

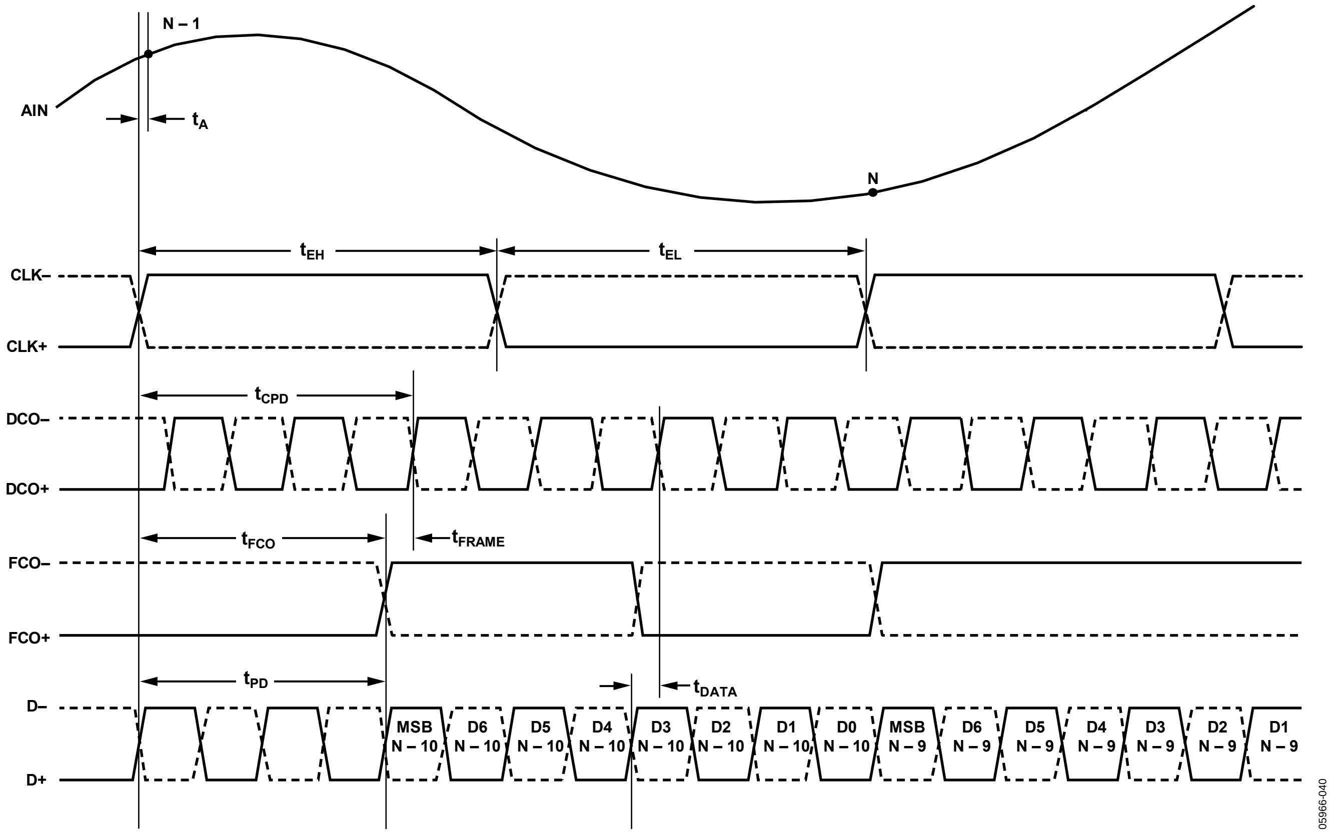


Figure 2. 8-Bit Data Serial Stream (Default)

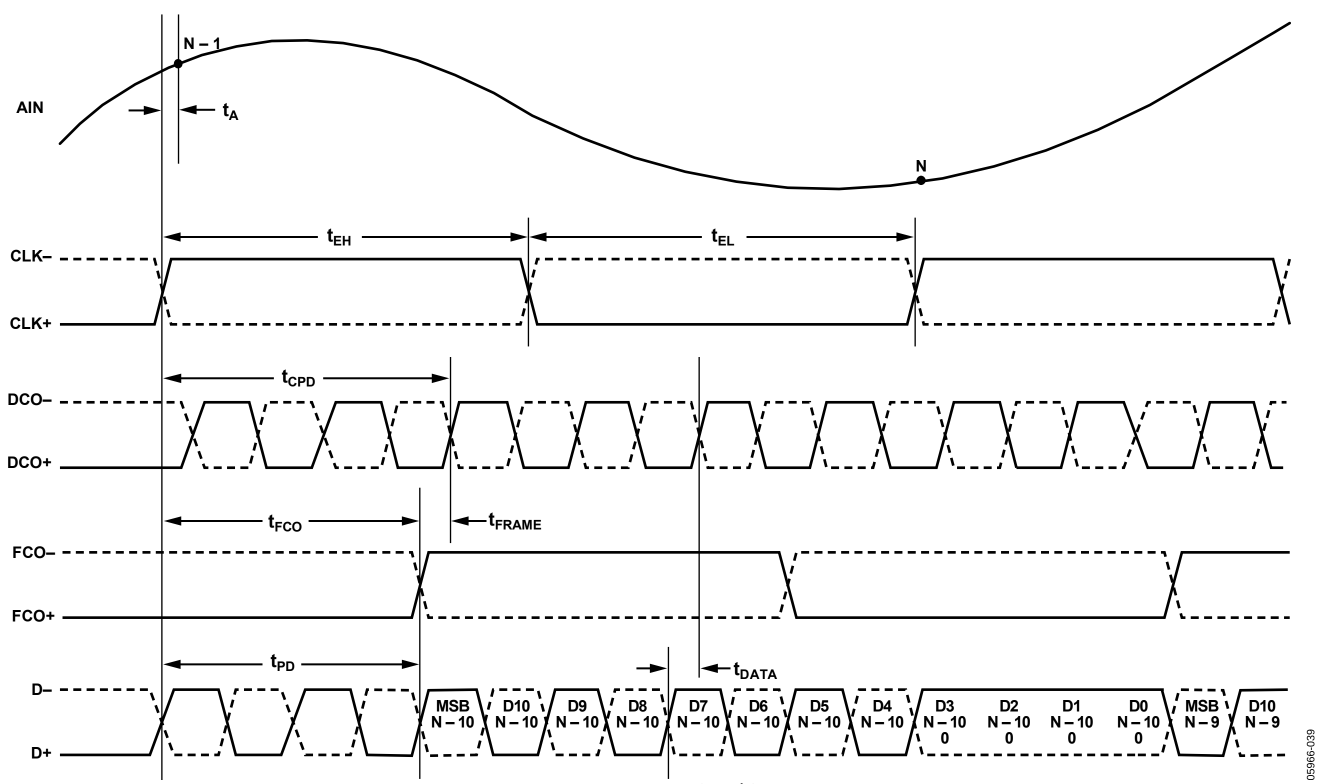


Figure 3. 12-Bit Data Serial Stream

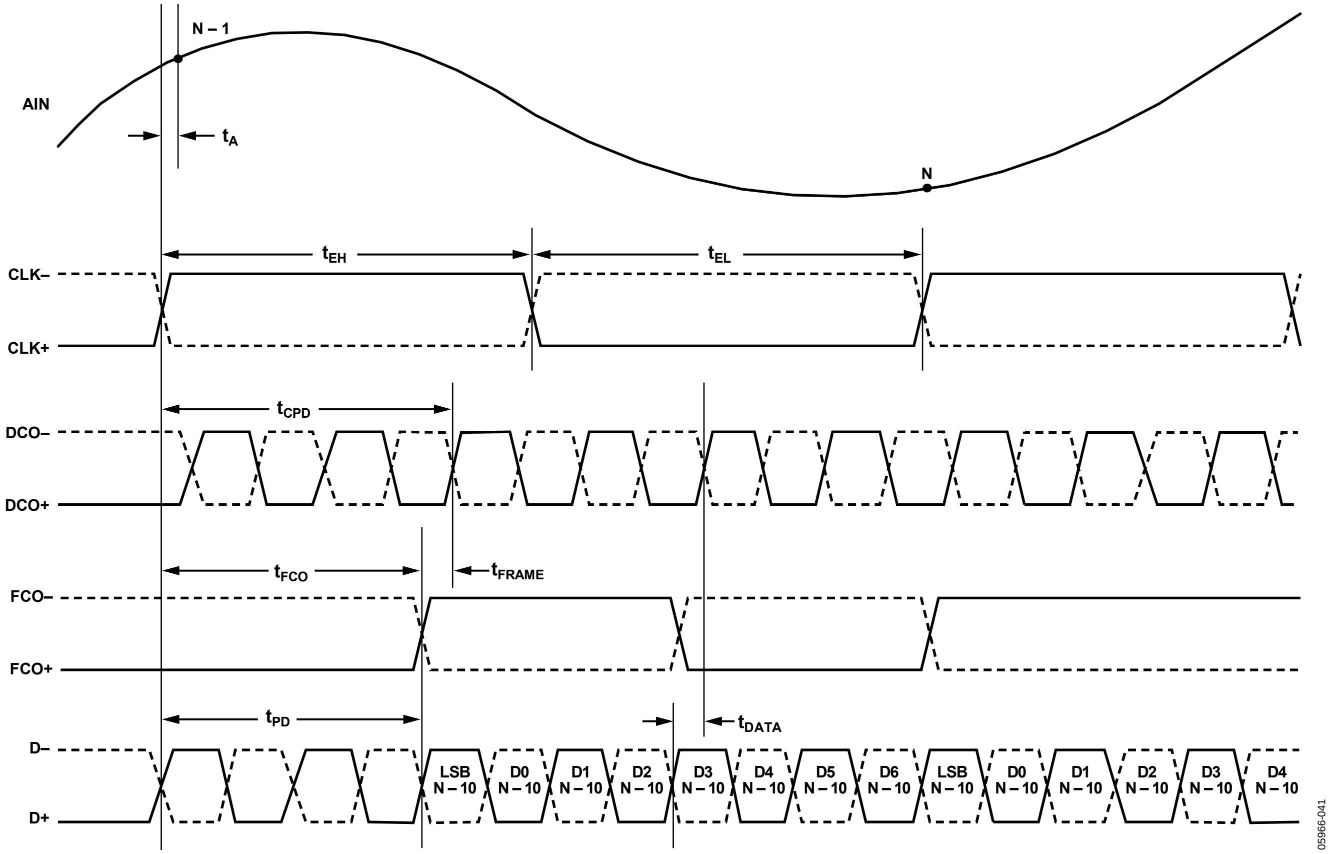


Figure 4. 8-Bit Data Serial Stream, LSB First

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect To	Rating
ELECTRICAL		
AVDD	AGND	−0.3 V to +2.0 V
DRVDD	DRGND	−0.3 V to +2.0 V
AGND	DRGND	−0.3 V to +0.3 V
AVDD	DRVDD	−2.0 V to +2.0 V
Digital Outputs (D+, D−, DCO+, DCO−, FCO+, FCO−)	DRGND	−0.3 V to +2.0 V
CLK+, CLK−	AGND	−0.3 V to +3.9 V
VIN+, VIN−	AGND	−0.3 V to +2.0 V
SDIO/ODM	AGND	−0.3 V to +2.0 V
PDWN, SCLK/DTP, CSB	AGND	−0.3 V to +3.9 V
REFT, REFB, RBIAS	AGND	−0.3 V to +2.0 V
VREF, SENSE	AGND	−0.3 V to +2.0 V
ENVIRONMENTAL		
Operating Temperature Range (Ambient)		−40°C to +85°C
Maximum Junction Temperature		150°C
Lead Temperature (Soldering, 10 sec)		300°C
Storage Temperature Range (Ambient)		−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE

Table 6.

Air Flow Velocity (m/s)	θ_{JA}[1]	θ_{JB}	θ_{JC}
0.0	24°C/W		
1.0	21°C/W	12.6°C/W	1.2°C/W
2.5	19°C/W		

[1] θ_{JA} for a 4-layer PCB with solid ground plane (simulated). Exposed pad soldered to PCB.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

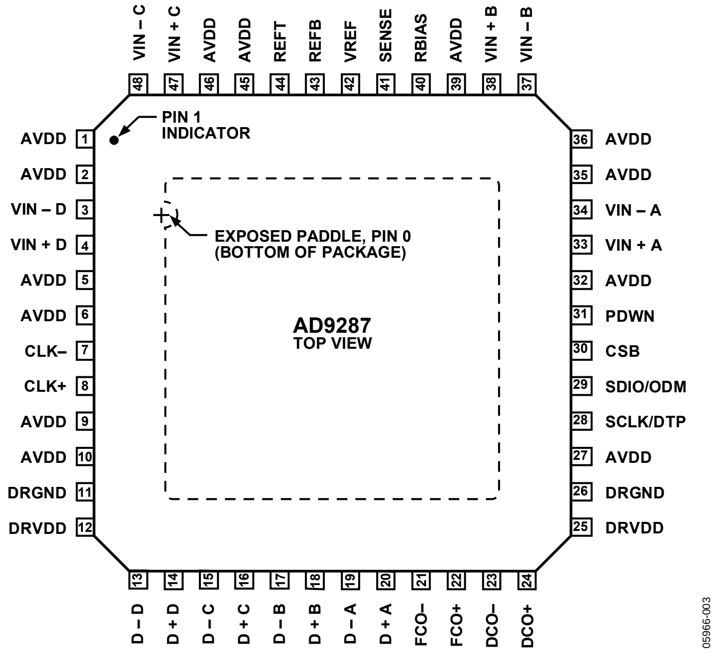


Figure 5. 48-Lead LFCSP Top View

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	AGND	Analog Ground (Exposed Paddle)
1, 2, 5, 6, 9, 10, 27, 32, 35, 36, 39, 45, 46	AVDD	1.8 V Analog Supply
11, 26	DRGND	Digital Output Driver Ground
12, 25	DRVDD	1.8 V Digital Output Driver Supply
3	VIN – D	ADC D Analog Input—Complement
4	VIN + D	ADC D Analog Input—True
7	CLK–	Input Clock—Complement
8	CLK+	Input Clock—True
13	D – D	ADC D Complement Digital Output
14	D + D	ADC D True Digital Output
15	D – C	ADC C Complement Digital Output
16	D + C	ADC C True Digital Output
17	D – B	ADC B Complement Digital Output
18	D + B	ADC B True Digital Output
19	D – A	ADC A Complement Digital Output
20	D + A	ADC A True Digital Output
21	FCO–	Frame Clock Output—Complement
22	FCO+	Frame Clock Output—True
23	DCO–	Data Clock Output—Complement
24	DCO+	Data Clock Output—True
28	SCLK/DTP	Serial Clock/Digital Test Pattern
29	SDIO/ODM	Serial Data Input-Output/Output Driver Mode
30	CSB	CSB
31	PDWN	Power-Down
33	VIN + A	ADC A Analog Input—True
34	VIN – A	ADC A Analog Input—Complement

Pin No.	Mnemonic	Description
37	VIN − B	ADC B Analog Input—Complement
38	VIN + B	ADC B Analog Input—True
40	RBIAS	External Resistor Sets the Internal ADC Core Bias Current
41	SENSE	Reference Mode Selection
42	VREF	Voltage Reference Input/Output
43	REFB	Differential Reference (Negative)
44	REFT	Differential Reference (Positive)
47	VIN + C	ADC C Analog Input—True
48	VIN − C	ADC C Analog Input—Complement

EQUIVALENT CIRCUITS

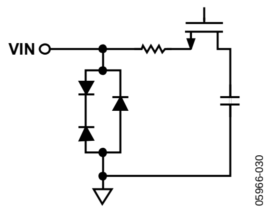


Figure 6. Equivalent Analog Input Circuit

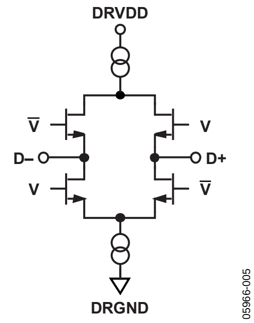


Figure 9. Equivalent Digital Output Circuit

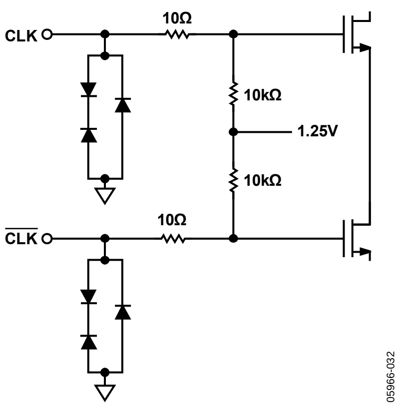


Figure 7. Equivalent Clock Input Circuit

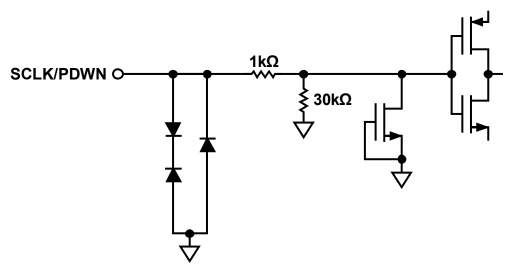


Figure 10. Equivalent SCLK/PDWN Input Circuit

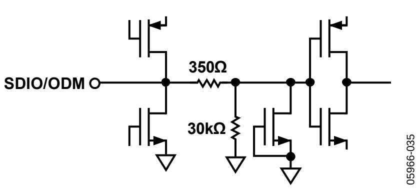


Figure 8. Equivalent SDIO/ODM Input Circuit

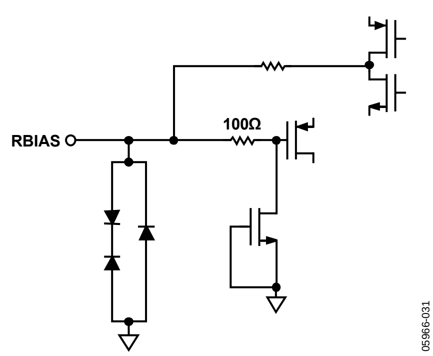


Figure 11. Equivalent RBIAS Circuit

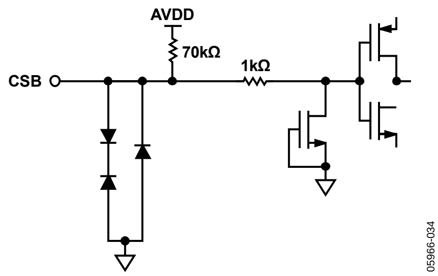


Figure 12. Equivalent CSB Input Circuit

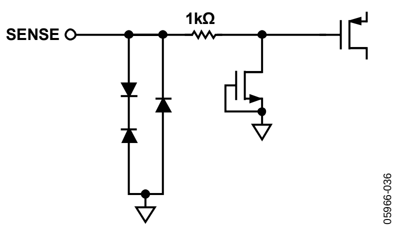


Figure 13. Equivalent SENSE Circuit

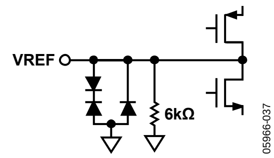


Figure 14. Equivalent VREF Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

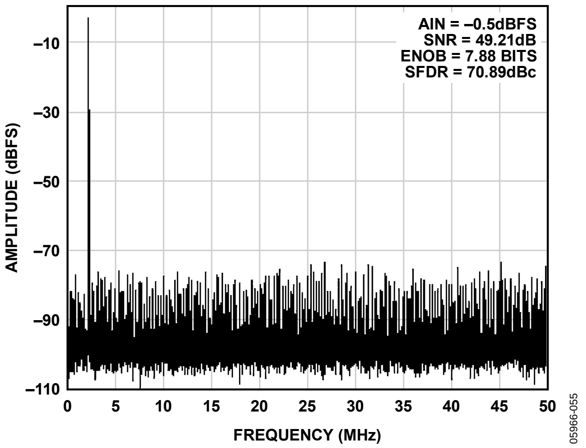


Figure 15. Single-Tone 32k FFT with f_{IN} = 2.3 MHz, f_{SAMPLE} = 100 MSPS

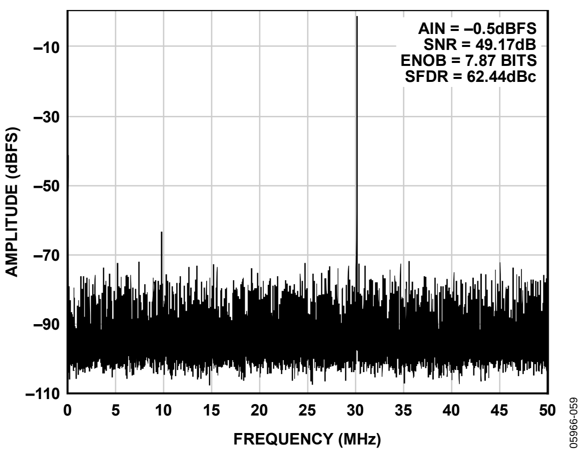


Figure 16. Single-Tone 32k FFT with f_{IN} = 70 MHz, f_{SAMPLE} = 100 MSPS

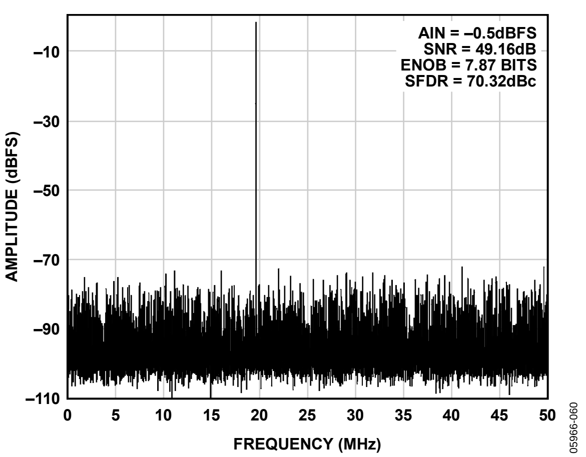


Figure 17. Single-Tone 32k FFT with f_{IN} = 120 MHz, f_{SAMPLE} = 100 MSPS

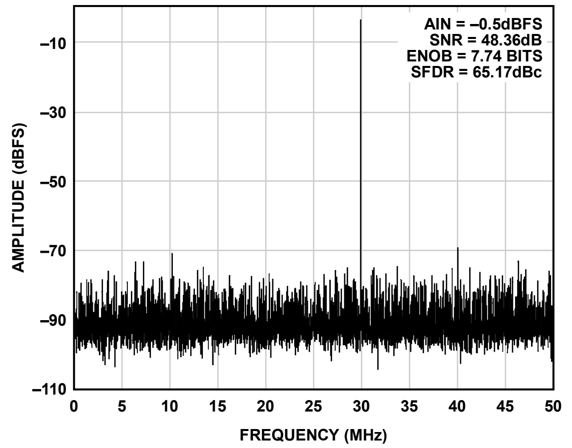


Figure 18. Single-Tone 32k FFT with f_{IN} = 170 MHz, f_{SAMPLE} = 100 MSPS

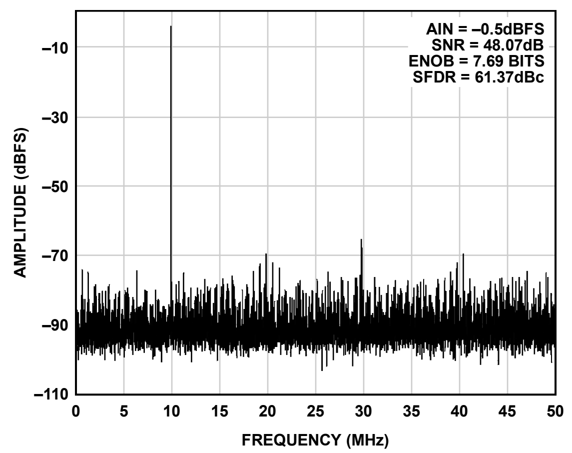


Figure 19. Single-Tone 32k FFT with f_{IN} = 190 MHz, f_{SAMPLE} = 100 MSPS

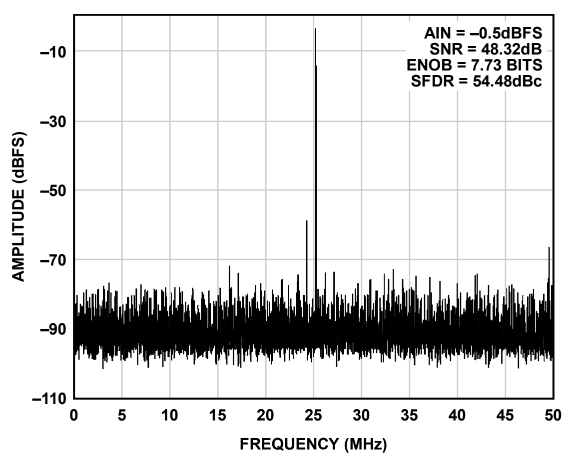


Figure 20. Single-Tone 32k FFT with f_{IN} = 225 MHz, f_{SAMPLE} = 100 MSPS

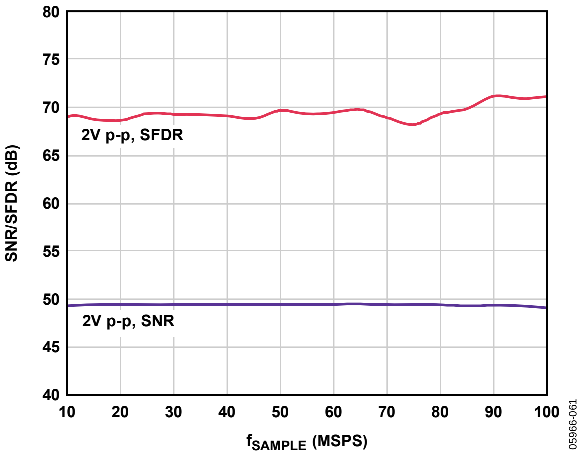


Figure 21. SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 10.3 MHz, f_{SAMPLE} = 100 MSPS

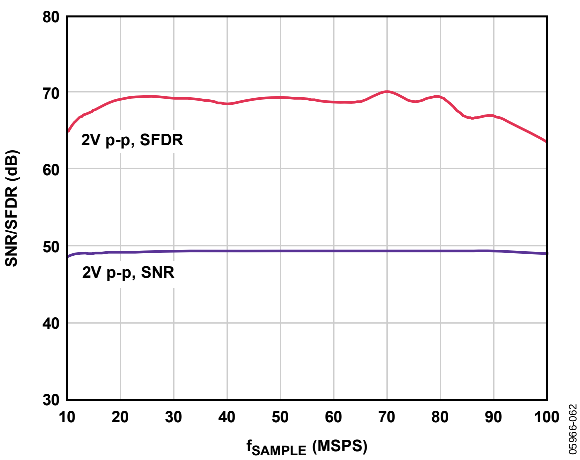


Figure 22. SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 35 MHz, f_{SAMPLE} = 100 MSPS

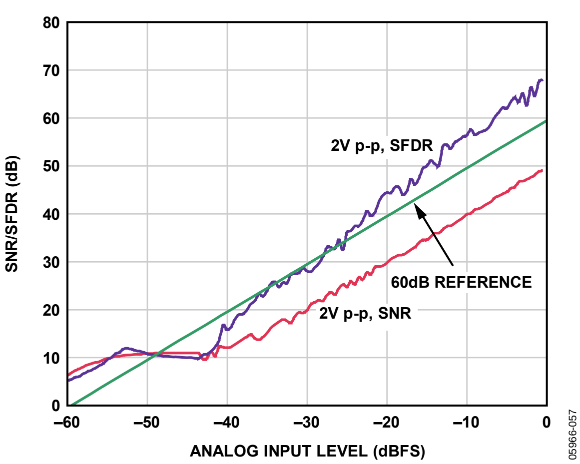


Figure 23. SNR/SFDR vs. Analog Input Level, f_{IN} = 10.3 MHz, f_{SAMPLE} = 100 MSPS

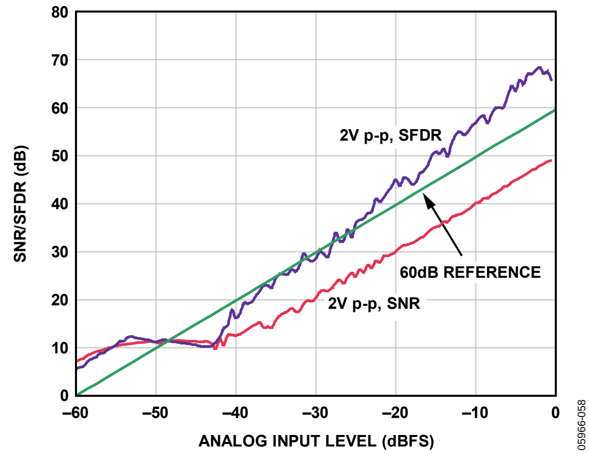


Figure 24. SNR/SFDR vs. Analog Input Level, f_{IN} = 35 MHz, f_{SAMPLE} = 100 MSPS

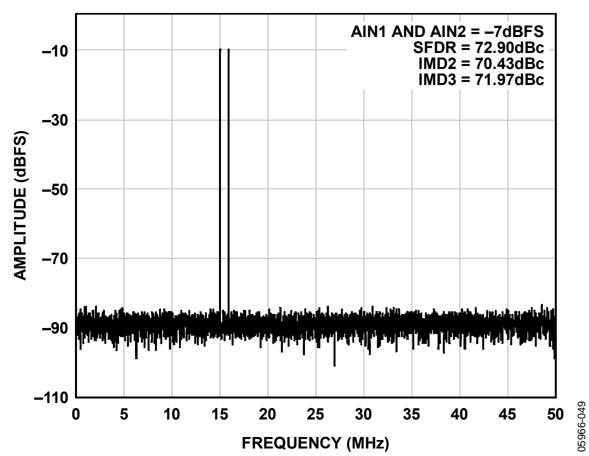


Figure 25. Two-Tone 32k FFT with f_{IN1} = 15 MHz and f_{IN2} = 16 MHz, f_{SAMPLE} = 100 MSPS

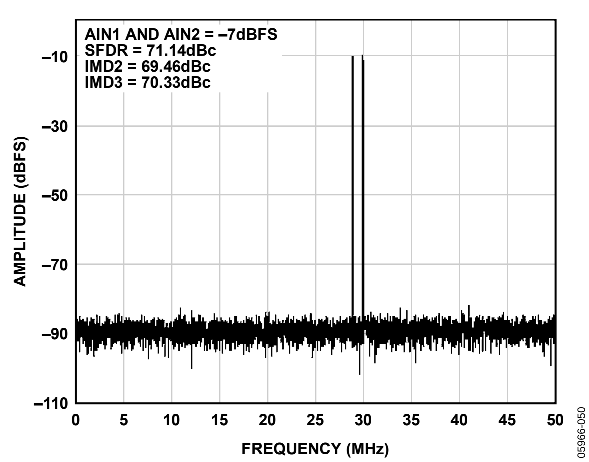


Figure 26. Two-Tone 32k FFT with f_{IN1} = 70 MHz and f_{IN2} = 71 MHz, f_{SAMPLE} = 100 MSPS

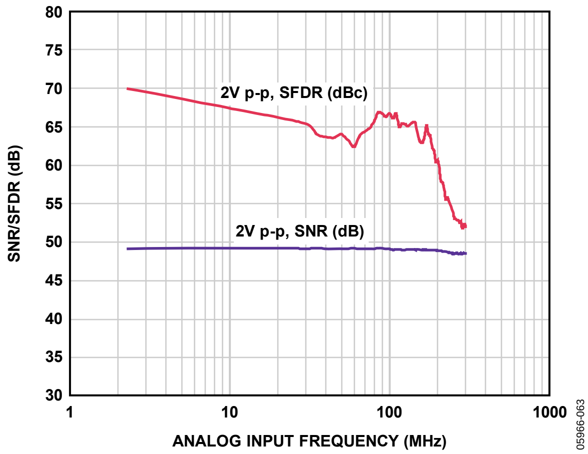


Figure 27. SNR/SFDR vs. f_{IN}, f_{SAMPLE} = 100 MSPS

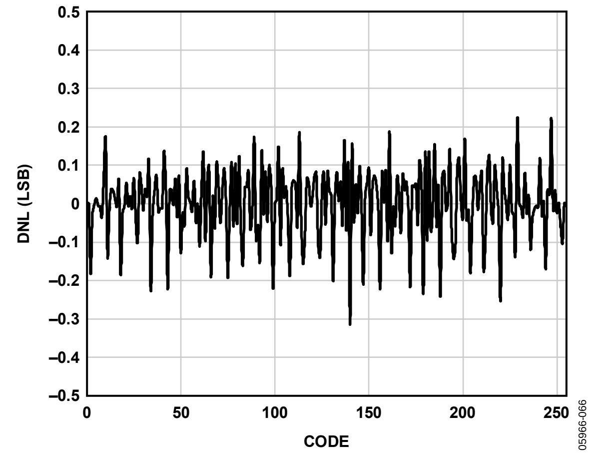


Figure 30. DNL, f_{IN} = 2.4 MHz, f_{SAMPLE} = 100 MSPS

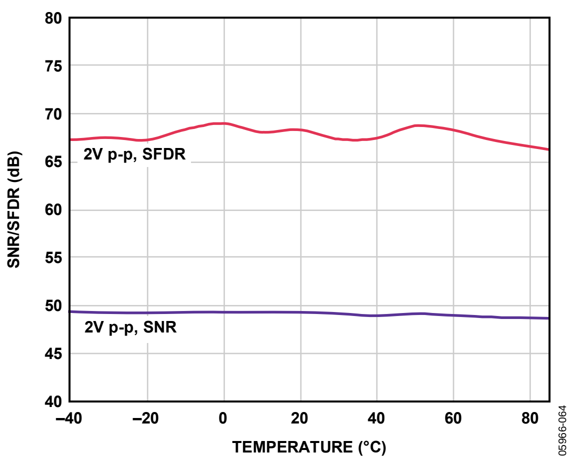


Figure 28. SINAD/SFDR vs. Temperature, f_{IN} = 10.3 MHz, f_{SAMPLE} = 100 MSPS

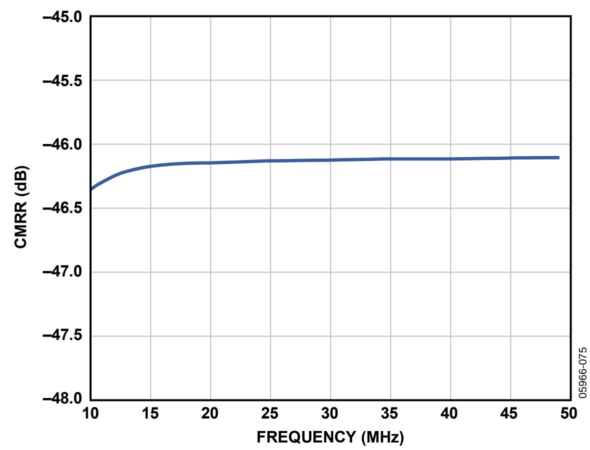


Figure 31. CMRR vs. Analog Input Frequency, f_{SAMPLE} = 100 MSPS

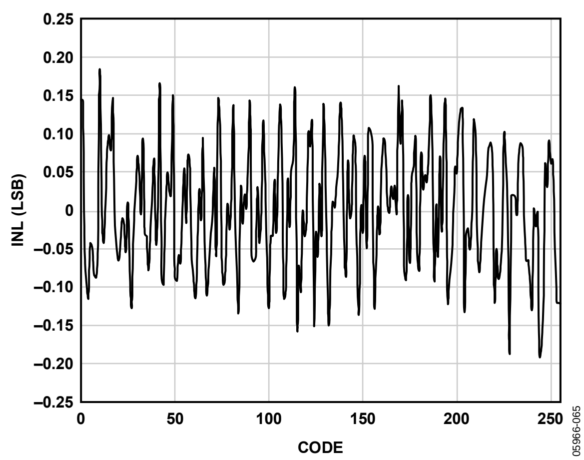


Figure 29. INL, f_{IN} = 2.4 MHz, f_{SAMPLE} = 100 MSPS

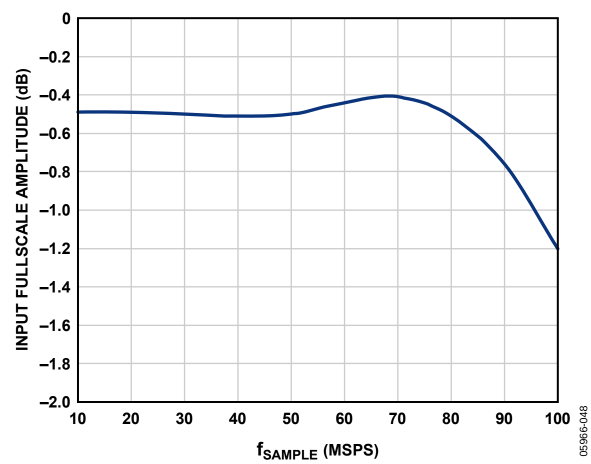


Figure 32. Input Full-Scale Amplitude vs. f_{SAMPLE}

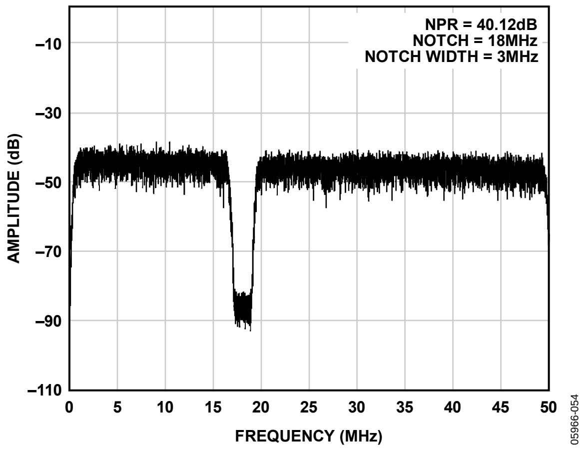


Figure 33. Noise Power Ratio (NPR), f_{SAMPLE} = 100 MSPS

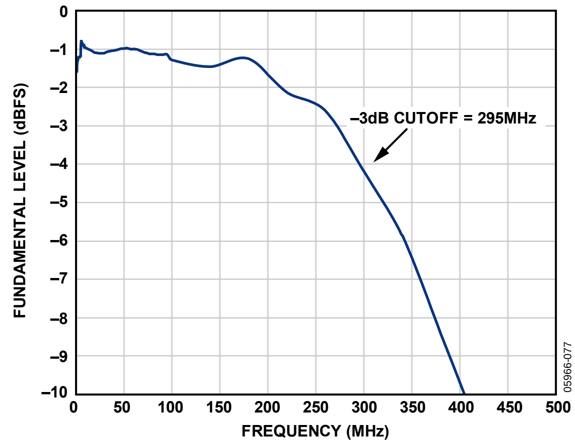


Figure 34. Full Power Bandwidth vs. Frequency, f_{SAMPLE} = 100 MSPS

THEORY OF OPERATION

The AD9287 architecture consists of a pipelined ADC that is divided into three sections: a 4-bit first stage followed by eight 1.5-bit stages and a final 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stages. The quantized outputs from each stage are combined into a final 8-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The data is then serialized and aligned to the frame and output clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9287 is a differential switched-capacitor circuit designed for processing differential input signals. The input can support a wide common-mode range and maintain excellent performance. An input common-mode voltage of midsupply minimizes signal-dependent errors and provides optimum performance.

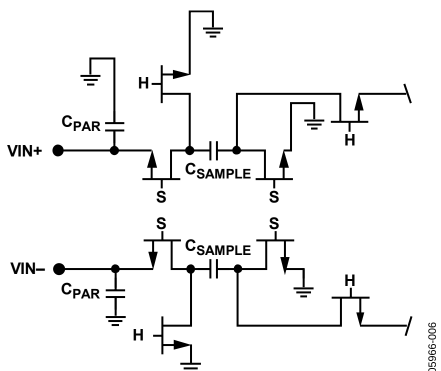


Figure 35. Switched-Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 35). When the input circuit is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. In addition, low-Q inductors or ferrite beads can be placed on each leg of the input to reduce the high differential capacitance seen at the analog inputs, thus realizing the maximum bandwidth of the ADC. Such use of low-Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a shunt capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit any unwanted broadband noise. See the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" for more information on this subject. In general, the precise values depend on the application.

The analog inputs of the AD9287 are not internally dc-biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that $V_{CM} = AVDD/2$ is recommended for optimum performance, but the device can function over a wider range with reasonable performance, as shown in Figure 36 and Figure 37.

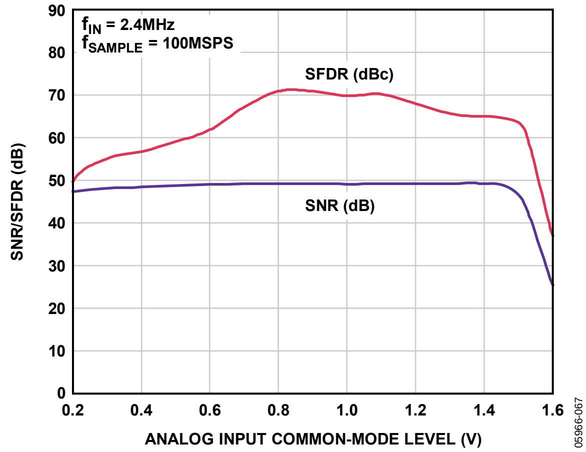


Figure 36. SNR/SFDR vs. Common-Mode Voltage, f_{IN} = 2.4 MHz, f_{SAMPLE} = 100 MSPS

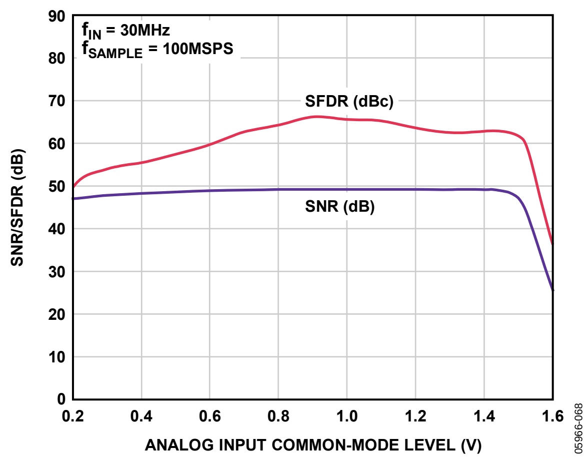


Figure 37. SNR/SFDR vs. Common-Mode Voltage, f_{IN} = 30 MHz, f_{SAMPLE} = 100 MSPS

For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates the positive and negative reference voltages, REFT and REFB, respectively, that define the span of the ADC core. The output common-mode of the reference buffer is set to midsupply, and the REFT and REFB voltages and span are defined as

$$REFT = 1/2\ (AVDD + VREF)$$
$$REFB = 1/2\ (AVDD - VREF)$$
$$Span = 2 \times (REFT - REFB) = 2 \times VREF$$

It can be seen from these equations that the REFT and REFB voltages are symmetrical about the midsupply voltage and, by definition, the input span is twice the value of the VREF voltage.

Maximum SNR performance is always achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9287, the largest input span available is 2 V p-p.

Differential Input Configurations

There are several ways in which to drive the AD9287 either actively or passively. In either case, the optimum performance is achieved by driving the analog input differentially. One example is by using the AD8332 differential driver. It provides excellent performance and a flexible interface to the ADC (see Figure 41) for baseband applications. This configuration is common for medical ultrasound systems.

However, the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9287. For applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. Two examples are shown in Figure 38 and Figure 39.

In any configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

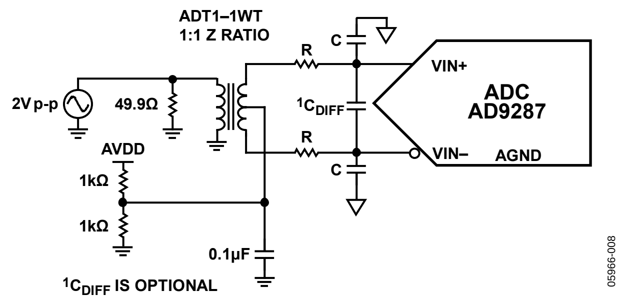


Figure 38. Differential Transformer Coupled Configuration for Baseband Applications

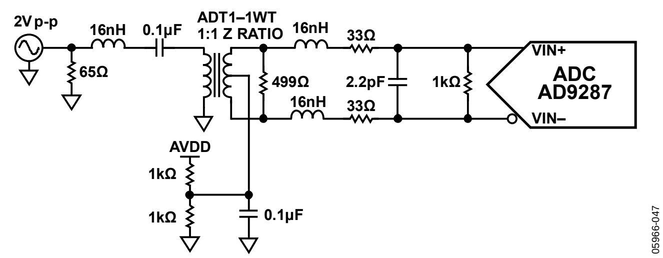


Figure 39. Differential Transformer Coupled Configuration for IF Applications

Single-Ended Input Configuration

A single-ended input may provide adequate performance in cost-sensitive applications. In this configuration, SFDR and distortion performance degrade due to the large input common-mode swing. If the application requires a single-ended input configuration, ensure that the source impedances on each input are well matched in order to achieve the best possible performance. A full-scale input of 2 V p-p can still be applied to the ADC's VIN+ pin while the VIN− pin is terminated. Figure 40 details a typical single-ended input configuration.

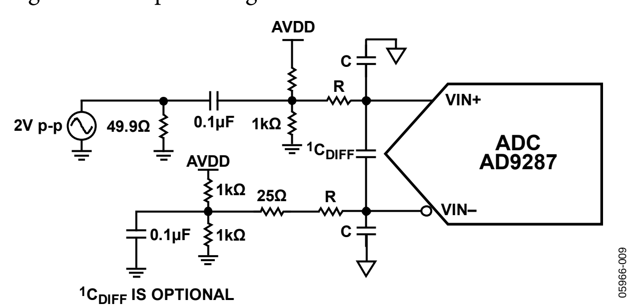


Figure 40. Single-Ended Input Configuration

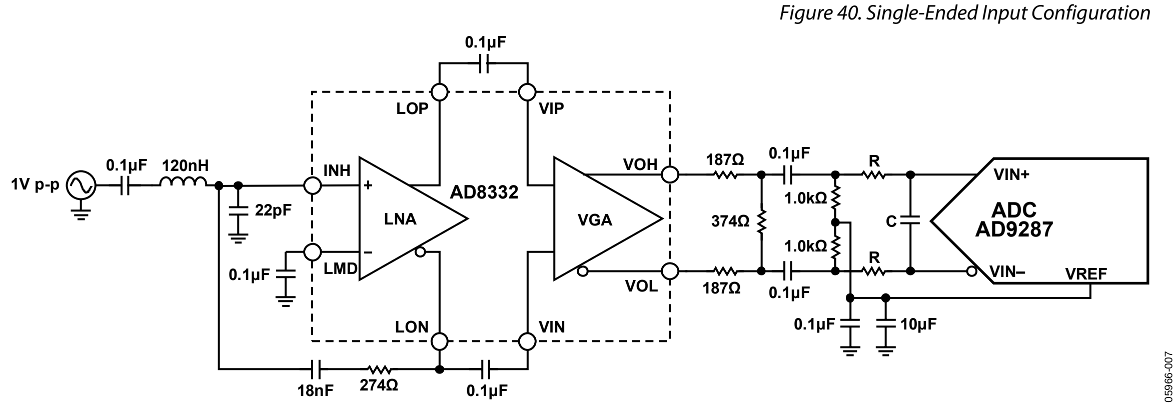


Figure 41. Differential Input Configuration Using the AD8332

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9287 sample clock inputs (CLK+ and CLK−) should be clocked with a differential signal. This signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or capacitors. These pins are biased internally and require no additional bias.

Figure 42 shows one preferred method for clocking the AD9287. The low jitter clock source is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock excursions into the AD9287 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9287 and preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

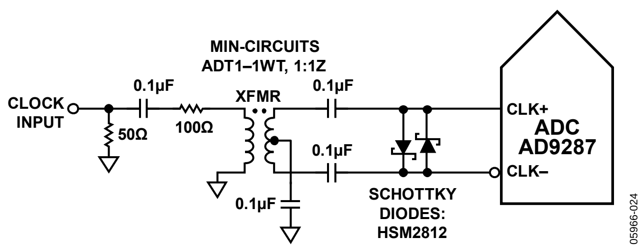


Figure 42. Transformer Coupled Differential Clock

If a low jitter clock is available, another option is to ac-couple a differential PECL signal to the sample clock input pins as shown in Figure 43. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515 family of clock drivers offers excellent jitter performance.

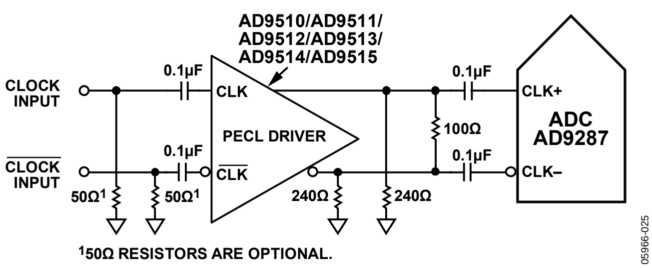


Figure 43. Differential PECL Sample Clock

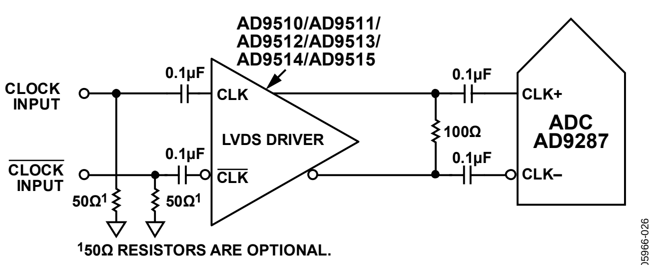


Figure 44. Differential LVDS Sample Clock

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, CLK+ should be directly driven from a CMOS gate, and the CLK− pin should be bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor (see Figure 45). Although the CLK+ input circuit supply is AVDD (1.8 V), this input is designed to withstand input voltages up to 3.3 V, making the selection of the drive logic voltage very flexible.

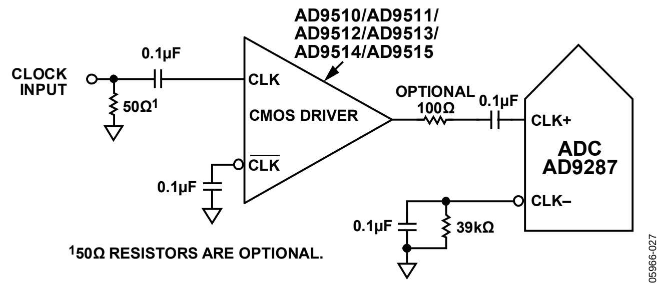


Figure 45. Single-Ended 1.8 V CMOS Sample Clock

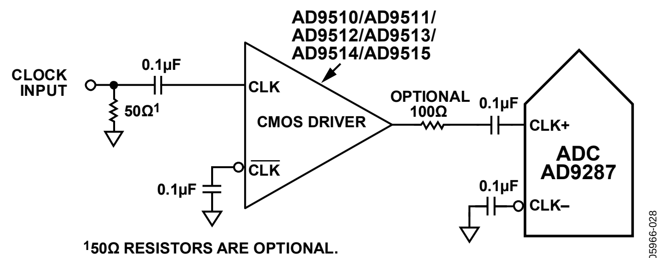


Figure 46. Single-Ended 3.3 V CMOS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9287 contains a duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9287. When the DCS is on, noise and distortion performance are nearly flat for a wide range of duty cycles. However, some applications may require the DCS function to be off. If so, keep in mind that the dynamic range performance can be affected when operated in this mode. See the Memory Map section for more details on using this feature.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately 10 clock cycles to allow the DLL to acquire and lock to the new rate.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR\ degradation = 20 \times \log 10\ [1/2 \times \pi \times f_A \times t_J]$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 47).

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9287. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs (visit www.analog.com).

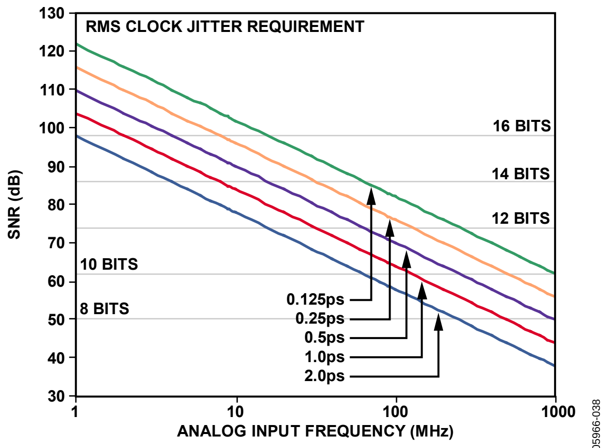


Figure 47. Ideal SNR vs. Input Frequency and Jitter

Power Dissipation and Power-Down Mode

As shown in Figure 48, the power dissipated by the AD9287 is proportional to its sample rate. The digital power dissipation does not vary much because it is determined primarily by the DRVDD supply and bias current of the LVDS output drivers.

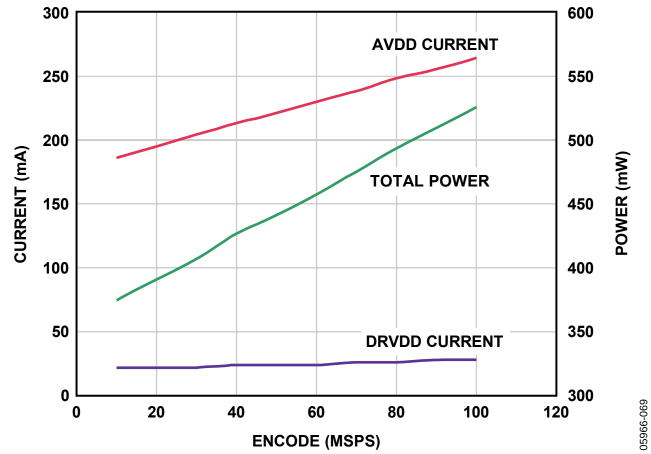


Figure 48. Supply Current vs. f_{SAMPLE} for f_{IN} = 10.3 MHz, f_{SAMPLE} = 100 MSPS

By asserting the PDWN pin high, the AD9287 is placed in power-down mode. In this state, the ADC typically dissipates 2 mW. During power-down, the LVDS output drivers are placed in a high impedance state. The AD9287 returns to normal operating mode when the PDWN pin is pulled low. This pin is both 1.8 V and 3.3 V tolerant.

In power-down mode, low power dissipation is achieved by shutting down the reference, reference buffer, PLL, and biasing networks. The decoupling capacitors on REFT and REFB are discharged when entering power-down mode and must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in the power-down mode; shorter cycles result in proportionally shorter wake-up times. With the recommended 0.1 μF and 2.2 μF decoupling capacitors on REFT and REFB, it takes approximately 1 sec to discharge the reference buffer decoupling capacitors fully and 375 μs to restore full operation.

There are a number of other power-down options available when using the SPI port interface. The user can individually power down each channel or put the entire device into standby mode. This allows the user to keep the internal PLL powered when fast wake-up times (~600 ns) are required. See the Memory Map section for more details on using these features.

Digital Outputs and Timing

The AD9287 differential outputs conform to the ANSI-644 LVDS standard on default power-up. This can be changed to a low power, reduced signal option similar to the IEEE 1596.3 standard using the SDIO/ODM pin or via the SPI. This LVDS standard can further reduce the overall power dissipation of the device by roughly 17 mW. See the SDIO/ODM Pin section or Table 15 in the Memory Map section for more information. The LVDS driver current is derived on-chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing at the receiver.

The AD9287 LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs that have LVDS capability for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as close to the receiver as possible. No far-end receiver termination and poor differential trace routing may result in timing errors. It is recommended that the trace length is no longer than 24 inches and that the differential output traces are kept close together and at equal lengths. An example of the FCO and data stream with proper trace length and position can be found in Figure 49.

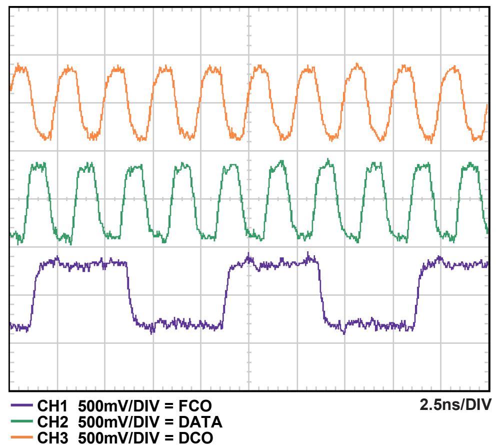


Figure 49. LVDS Output Timing Example in ANSI Mode (Default)

An example of the LVDS output using the ANSI standard (default) data eye and a time interval error (TIE) jitter histogram with trace lengths less than 24 inches on regular FR-4 material is shown in Figure 50. Figure 51 shows an example of when the trace lengths exceed 24 inches on regular FR-4 material. Notice that the TIE jitter histogram reflects the decrease of the data eye opening as the edge deviates from the ideal position. It is up to the user to determine if the waveforms meet the timing budget of the design when the trace lengths exceed 24 inches. Additional SPI options allow the user to further increase the internal termination (increasing the current) of all four outputs in order to drive longer trace lengths (see Figure 52). Even though this produces sharper rise and fall times on the data edges and is less prone to bit errors, the power dissipation of the DRVDD supply increases when this option is used. Also notice in Figure 52 that the histogram has improved. See the Memory Map section for more details.

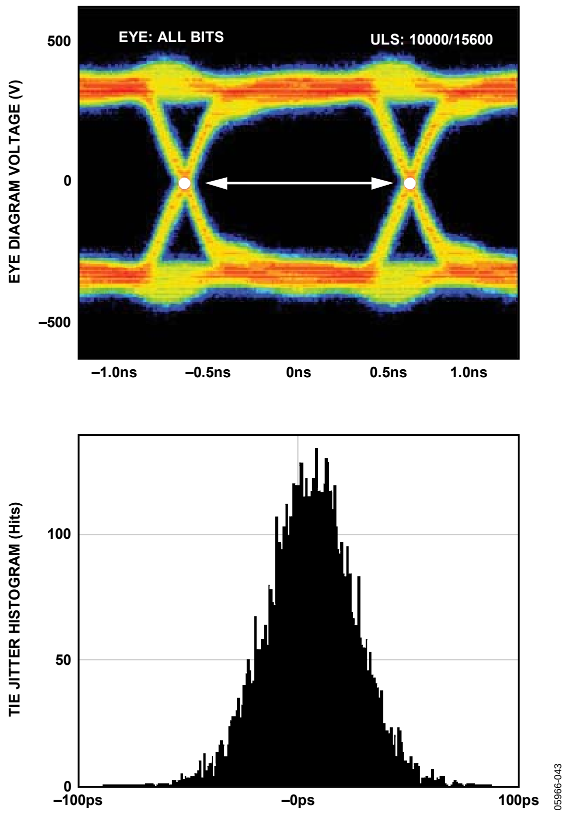


Figure 50. Data Eye for LVDS Outputs in ANSI Mode with Trace Lengths Less than 24 Inches on Standard FR-4

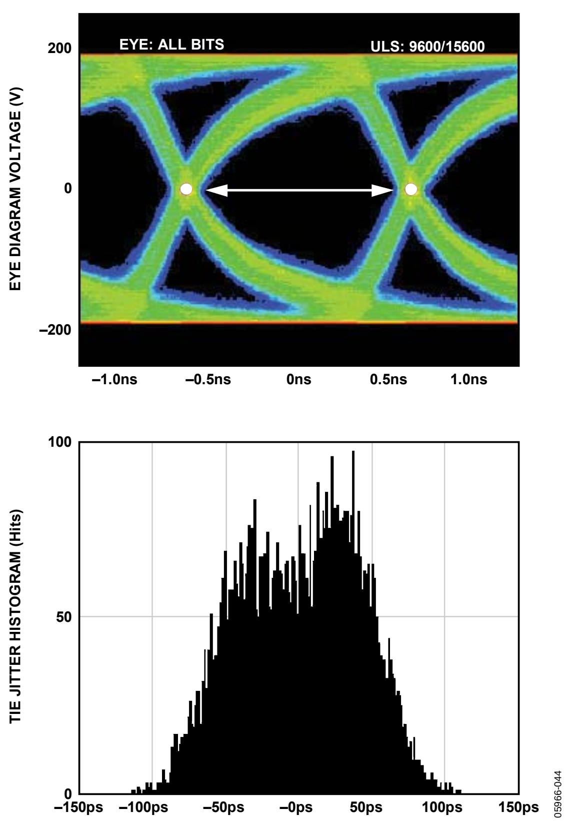


Figure 51. Data Eye for LVDS Outputs in ANSI Mode with Trace Lengths Greater than 24 Inches on Standard FR-4

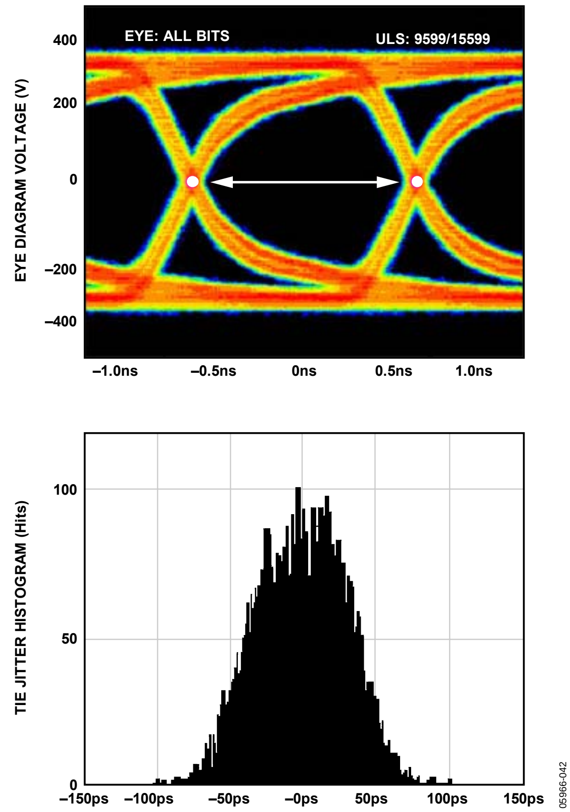


Figure 52. Data Eye for LVDS Outputs in ANSI Mode with 100 Ω Termination on and Trace Lengths Greater than 24 Inches on Standard FR-4

The format of the output data is offset binary by default. An example of the output coding format can be found in Table 8. If it is desired to change the output data format to twos complement, see the Memory Map section.

Table 8. Digital Output Coding

Code	(VIN+) − (VIN−), Input Span = 2 V p-p (V)	Digital Output Offset Binary (D11 ... D0)
255	+1.00	1111 1111
128	0.00	1000 0000
127	−0.007813	0111 1111
0	−1.00	0000 0000

Data from each ADC is serialized and provided on a separate channel. The data rate for each serial stream is equal to 8 bits times the sample clock rate, with a maximum of 800 Mbps (8 bits × 100 MSPS = 800 Mbps). The lowest typical conversion rate is 10 MSPS. However, if lower sample rates are required for a specific application, the PLL can be set up for encode rates lower than 10 MSPS via the SPI. This allows encode rates as low as 5 MSPS. See the Memory Map section to enable this feature.

Two output clocks are provided to assist in capturing data from the AD9287. The DCO is used to clock the output data and is equal to four times the sampling clock (CLK) rate. Data is clocked out of the AD9287 and must be captured on the rising and falling edges of the DCO that supports double data rate (DDR) capturing. The frame clock out (FCO) is used to signal the start of a new output byte and is equal to the sampling clock rate. See the timing diagram shown in Figure 2 for more information.

Table 9. Flex Output Test Modes

Output Test Mode Bit Sequence	Pattern Name	Digital Output Word 1	Digital Output Word 2	Subject to Data Format Select
0000	OFF (default)	N/A	N/A	N/A
0001	Midscale Short	1000 0000 (8-bit) 10 0000 0000 (10-bit) 1000 0000 0000 (12-bit) 10 0000 0000 0000 (14-bit)	Same	Yes
0010	+Full-Scale Short	1111 1111 (8-bit) 11 1111 1111 (10-bit) 1111 1111 1111 (12-bit) 11 1111 1111 1111 (14-bit)	Same	Yes
0011	−Full-Scale Short	0000 0000 (8-bit) 00 0000 0000 (10-bit) 0000 0000 0000 (12-bit) 00 0000 0000 0000 (14-bit)	Same	Yes
0100	Checker Board	1010 1010 (8-bit) 10 1010 1010 (10-bit) 1010 1010 1010 (12-bit) 10 1010 1010 1010 (14-bit)	0101 0101 (8-bit) 01 0101 0101 (10-bit) 0101 0101 0101 (12-bit) 01 0101 0101 0101 (14-bit)	No
0101	PN Sequence Long[1]	N/A	N/A	Yes
0110	PN Sequence Short[1]	N/A	N/A	Yes
0111	One/Zero Word Toggle	1111 1111 (8-bit) 11 1111 1111 (10-bit) 1111 1111 1111 (12-bit) 11 1111 1111 1111 (14-bit)	0000 0000 (8-bit) 00 0000 0000 (10-bit) 0000 0000 0000 (12-bit) 00 0000 0000 0000 (14-bit)	No
1000	User Input	Register 0x19 to Register 0x1A	Register 0x1B to Register 0x1C	No
1001	One/Zero Bit Toggle	1010 1010 (8-bit) 10 1010 1010 (10-bit) 1010 1010 1010 (12-bit) 10 1010 1010 1010 (14-bit)	N/A	No
1010	1× Sync	0000 1111 (8-bit) 00 0001 1111 (10-bit) 0000 0011 1111 (12-bit) 00 0000 0111 1111 (14-bit)	N/A	No
1011	One Bit High	1000 0000 (8-bit) 10 0000 0000 (10-bit) 1000 0000 0000 (12-bit) 10 0000 0000 0000 (14-bit)	N/A	No
1100	Mixed Frequency	1010 0011 (8-bit) 10 0110 0011 (10-bit) 1010 0011 0011 (12-bit) 10 1000 0110 0111 (14-bit)	N/A	No

[1] PN, or pseudorandom number, sequence is determined by the number of bits in the shift register. The long sequence is 23 bits and the short sequence is 9 bits. How the sequence is generated and utilized is described in the ITU O.150 standard. In general, the polynomial, X23 + X18 + 1 (long) and X9 + X5 + 1 (short), defines the pseudorandom sequence.

When using the serial port interface (SPI), the DCO phase can be adjusted in 60° increments relative to the data edge. This enables the user to refine system timing margins if required. The default DCO timing, as shown in Figure 2, is 90° relative to the output data edge.

A 10-, 12-, and 14-bit serial stream can also be initiated from the SPI. This allows the user to implement and test compatibility to higher resolution systems. However, when using the 12-bit option, the data stream stuffs four 0s at the end of the normal 12-bit serial data. See Figure 3 for a 12-bit example.

When using the SPI, all of the data outputs can also be inverted from their nominal state. This is not to be confused with inverting the serial stream to an LSB-first mode. In default mode, as shown in Figure 2, the MSB is represented first in the data output serial stream. However, this can be inverted so that the LSB is represented first in the data output serial stream (see Figure 4).

There are 12 digital output test pattern options available that can be initiated through the SPI. This is a useful feature when validating receiver capture and timing. Refer to Table 9 for the output bit sequencing options available. Some test patterns have two serial sequential words and can be alternated in various ways, depending on the test pattern chosen. It should be noted that some patterns may not adhere to the data format select option. In addition, customer user patterns can be assigned in the 0x19, 0x1A, 0x1B, and 0x1C register addresses. All test mode options can support 8- to 14-bit word lengths in order to verify data capture to the receiver.

Please consult the Memory Map section for information on how to change these additional digital output timing features through the serial port interface or SPI.

SDIO/ODM Pin

This pin is for applications that do not require SPI mode operation. The SDIO/ODM pin can enable a low power, reduced signal option similar to the IEEE 1596.3 reduced range link output standard if this pin and the CSB pin are tied to AVDD during device power-up. This option should only be used when the digital output trace lengths are less than 2 inches in length to the LVDS receiver. The FCO, DCO, and outputs still work as usual, but the LVDS signal swing of all channels is reduced from 350 mV p-p to 200 mV p-p. This output mode allows the user to further lower the power on the DRVDD supply. For applications where this pin is not used, it should be tied low. In this case, the device pin can be left open, and the 30 kΩ internal pull-down resistor pulls this pin low. This pin is only 1.8 V tolerant. If applications require this pin to be driven from a 3.3 V logic level, insert a 1 kΩ resistor in series with this pin to limit the current.

Table 10. Output Driver Mode Pin Settings

Selected ODM	ODM Voltage	Resulting Output Standard	Resulting FCO and DCO
Normal operation	10 kΩ to AGND	ANSI-644 (default)	ANSI-644 (default)
ODM	AVDD	Low power, reduced signal option	Low power, reduced signal option

SCLK/DTP Pin

This pin is for applications that do not require SPI mode operation. The serial clock/digital test pattern (SCLK/DTP) pin can enable a single digital test pattern if this pin and the CSB pin are held high during device power-up. When the DTP is tied to AVDD, all the ADC channel outputs shift out the following pattern: 1000 0000. The FCO and DCO outputs still work as usual while all channels shift out the repeatable test pattern. This pattern allows the user to perform timing alignment adjustments among the FCO, DCO, and output data. For normal operation, this pin should be tied to AGND through a 10 kΩ resistor. This pin is both 1.8 V and 3.3 V tolerant.

Table 11. Digital Test Pattern Pin Settings

Selected DTP	DTP Voltage	Resulting D+ and D−	Resulting FCO and DCO
Normal operation	10 kΩ to AGND	Normal operation	Normal operation
DTP	AVDD	1000 0000	Normal operation

Additional and custom test patterns can also be observed when commanded from the SPI port. Consult the Memory Map section to choose from the different options available.

CSB Pin

The chip select bar (CSB) pin should be tied to AVDD for applications that do not require SPI mode operation. By tying CSB high, all SCLK and SDIO information is ignored. This pin is both 1.8 V and 3.3 V tolerant.

RBIAS Pin

To set the internal core bias current of the ADC, place a resistor (nominally equal to 10.0 kΩ) to ground at the RBIAS pin. The resistor current is derived on-chip and sets the ADC's AVDD current to a nominal 260 mA at 100 MSPS. Therefore, it is imperative that at least a 1% tolerance on this resistor be used to achieve consistent performance. If SFDR performance is not as critical as power, simply adjust the ADC core current to achieve a lower power. Figure 53 and Figure 54 show the relationship between the dynamic range and power as the RBIAS resistance is changed. Nominally, we use a 10.0 kΩ value, as indicated by the dashed line.

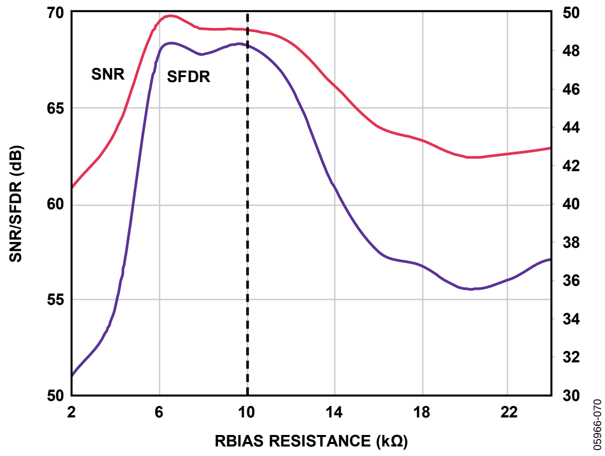


Figure 53. SFDR vs. RBIAS Resistance

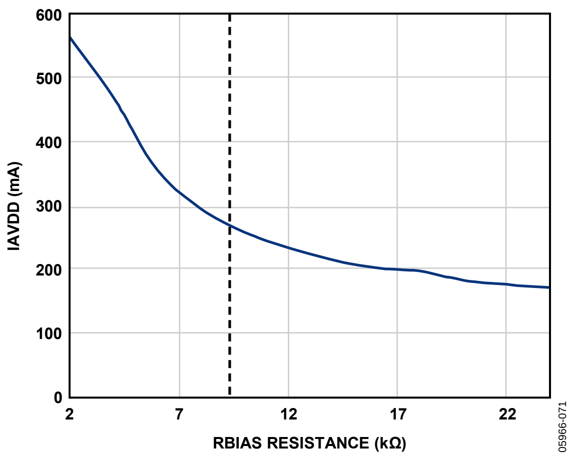


Figure 54. IAVDD vs. RBIAS Resistance

Voltage Reference

A stable and accurate 0.5 V voltage reference is built into the AD9287. This is gained up by a factor of 2 internally, setting V_{REF} to 1.0 V, which results in a full-scale differential input span of 2 V p-p. The V_{REF} is set internally by default; however, the VREF pin can be driven externally with a 1.0 V reference to achieve more accuracy.

When applying the decoupling capacitors to the VREF, REFT, and REFB pins, use ceramic low ESR capacitors. These capacitors should be close to the ADC pins and on the same layer of the PCB as the AD9287. The recommended capacitor values and configurations for the AD9287 reference pin can be found in Figure 55.

Table 12. Reference Settings

Selected Mode	SENSE Voltage	Resulting VREF (V)	Resulting Differential Span (V p-p)
External Reference	AVDD	N/A	2 × external reference
Internal, 2 V p-p FSR	AGND to 0.2 V	1.0	2.0

Internal Reference Operation

A comparator within the AD9287 detects the potential at the SENSE pin and configures the reference. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 55), setting VREF to 1 V.

The REFT and REFB pins establish their input span of the ADC core from the reference configuration. The analog input full-scale range of the ADC equals twice the voltage at the reference pin for either an internal or an external reference configuration.

If the reference of the AD9287 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 57 depicts how the internal reference voltage is affected by loading.

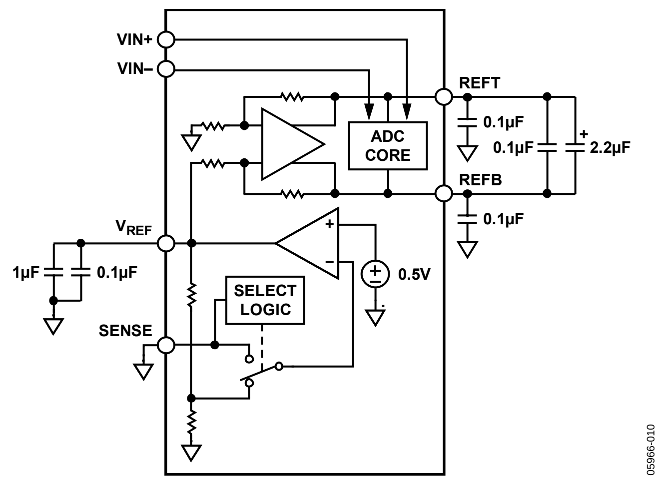
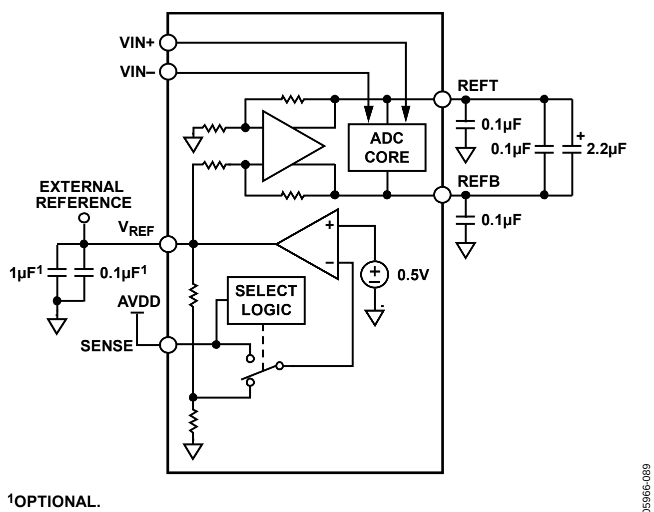


Figure 55. Internal Reference Configuration



[1]OPTIONAL.

Figure 56. External Reference Operation

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 58 shows the typical drift characteristics of the internal reference in 1 V mode.

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. The external reference is loaded with an equivalent 6 kΩ load. An internal reference buffer generates the positive and negative full-scale references, REFT and REFB, for the ADC core. Therefore, the external reference must be limited to a nominal of 1.0 V.

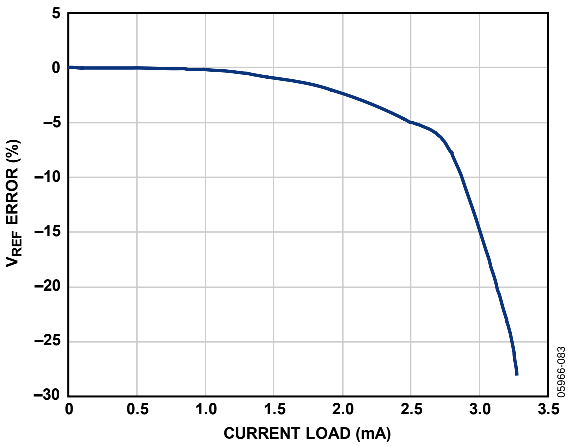


Figure 57. V_{REF} Error vs. Load

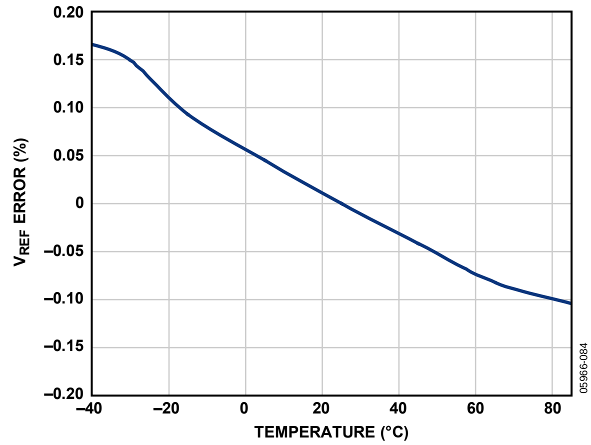


Figure 58. V_{REF} Error vs. Temperature

SERIAL PORT INTERFACE (SPI)

The AD9287 serial port interface allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. This gives the user added flexibility and customization depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided down into fields, as documented in the Memory Map section. Detailed operational information can be found in the Analog Devices user manual *Interfacing to High Speed ADCs via SPI*.

There are three pins that define the serial port interface or SPI to this particular ADC. They are the SCLK, SDIO, and CSB pins. The SCLK (serial clock) is used to synchronize the read and write data presented to the ADC. The SDIO (serial data input/output) is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. The CSB (chip select bar) is an active low control that enables or disables the read and write cycles (see Table 13).

Table 13. Serial Port Pins

Pin	Function
SCLK	Serial Clock. The serial shift clock in. SCLK is used to synchronize serial interface reads and writes.
SDIO	Serial Data Input/Output. A dual-purpose pin. The typical role for this pin is an input or output, depending on the instruction sent and the relative position in the timing frame.
CSB	Chip Select Bar (Active Low). This control gates the read and write cycles.

The falling edge of the CSB in conjunction with the rising edge of the SCLK determines the start of the framing sequence. During an instruction phase, a 16-bit instruction is transmitted followed by one or more data bytes, which is determined by Bit Fields W0 and W1. An example of the serial timing and its definitions can be found in Figure 59 and Table 14. In normal operation, CSB is used to signal to the device that SPI commands are to be received and processed. When CSB is brought low, the device processes SCLK and SDIO to process instructions. Normally, CSB remains low until the communication cycle is complete. However, if connected to a slow device, CSB can be brought high between bytes, allowing old microcontrollers enough time to transfer data into shift registers. CSB can be stalled when transferring one, two, or three bytes of data. When W0 and W1 are set to 11, the device enters streaming mode and continues to process data, either reading or writing, until the CSB is taken high to end the communication cycle. This allows complete memory transfers without having to provide additional instructions. Regardless of the mode, if CSB is taken high in the middle of any byte transfer, the SPI state machine is reset and the device waits for a new instruction.

In addition to the operation modes, the SPI port can be configured to operate in different manners. For applications that do not require a control port, the CSB line can be tied and held high. This places the remainder of the SPI pins in their secondary mode as defined in the Serial Port Interface (SPI) section. CSB can also be tied low to enable 2-wire mode. When CSB is tied low, SCLK and SDIO are the only pins required for communication. Although the device is synchronized during power-up, caution must be exercised when using this mode to ensure that the serial port remains synchronized with the CSB line. When operating in 2-wire mode, it is recommended to use a 1-, 2-, or 3-byte transfer exclusively. Without an active CSB line, streaming mode can be entered but not exited.

In addition to word length, the instruction phase determines if the serial frame is a read or write operation, allowing the serial port to be used to both program the chip and read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB- or LSB-first mode. MSB-first mode is the default at power-up and can be changed by adjusting the configuration register. For more information about this and other features, see the user manual *Interfacing to High Speed ADCs via SPI*.

HARDWARE INTERFACE

The pins described in Table 13 compose the physical interface between the user's programming device and the serial port of the AD9287. The SCLK and CSB pins function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

This interface is flexible enough to be controlled by either serial PROMS or PIC mirocontrollers. This provides the user an alternative method, other than a full SPI controller, to program the ADC (see the AN-812 Application Note).

If the user chooses not to use the SPI interface, these pins serve a dual function and are associated with secondary functions when the CSB is strapped to AVDD during device power-up. See the Theory of Operation section for details on which pin-strappable functions are supported on the SPI pins.

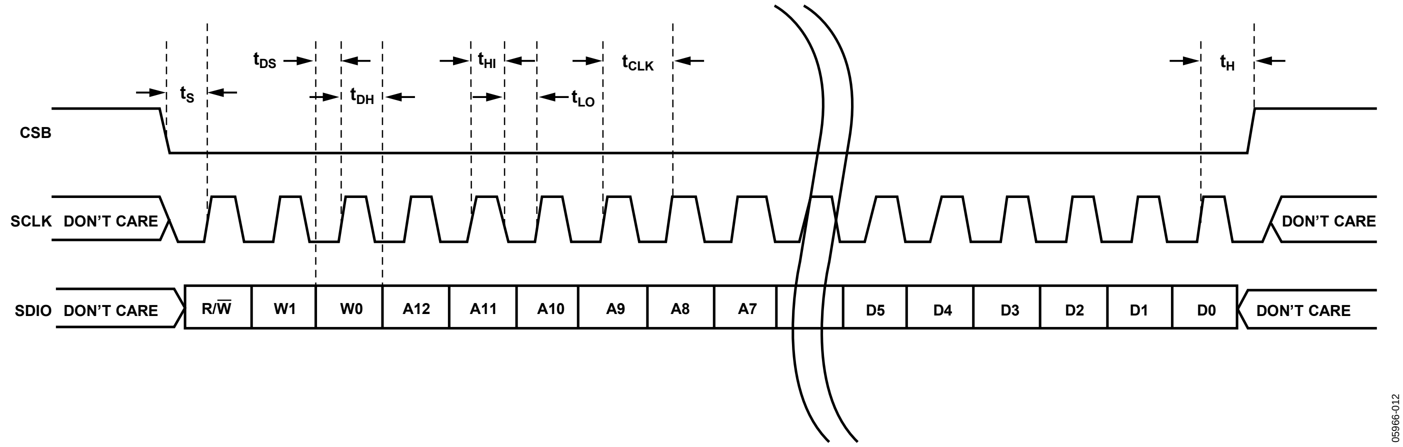


Figure 59. Serial Timing Details

Table 14. Serial Timing Definitions

Parameter	Timing (minimum, ns)	Description
t_{DS}	5	Set-up time between the data and the rising edge of SCLK
t_{DH}	2	Hold time between the data and the rising edge of SCLK
t_{CLK}	40	Period of the clock
t_S	5	Set-up time between CSB and SCLK
t_H	2	Hold time between CSB and SCLK
t_{HI}	16	Minimum period that SCLK should be in a logic high state
t_{LO}	16	Minimum period that SCLK should be in a logic low state

MEMORY MAP

READING THE MEMORY MAP TABLE

Each row in the memory map table has eight address locations. The memory map is roughly divided into three sections: chip configuration register map (Address 0x00 to Address 0x02), device index and transfer register map (Address 0x05 and Address 0xFF), and program register map (Address 0x08 to Address 0x25).

The left-hand column of the memory map indicates the register address number in hexadecimal. The default value of this address is shown in hexadecimal in the right-hand column. The Bit 7 (MSB) column is the start of the default hexadecimal value given. For example, Hexadecimal Address 0x09, Clock, has a hexadecimal default value of 0x01. This means Bit 7 = 0, Bit 6 = 0, Bit 5 = 0, Bit 4 = 0, Bit 3 = 0, Bit 2 = 0, Bit 1 = 0, and Bit 0 = 1, or 0000 0001 in binary. This setting is the default for the duty cycle stabilizer in the on condition. By writing a 0 to Bit 6 at this address, the duty cycle stabilizer turns off. For more information on this and other functions, consult the user manual *Interfacing to High Speed ADCs via SPI*.

RESERVED LOCATIONS

Undefined memory locations should not be written to except when writing the default values suggested in this data sheet. Addresses that have values marked as 0 should be considered reserved and have a 0 written into their registers during power-up.

DEFAULT VALUES

Coming out of reset, critical registers are preloaded with default values. These values are indicated in Table 15, where an X refers to an undefined feature.

LOGIC LEVELS

An explanation of various registers follows: “Bit is set” is synonymous with “bit is set to Logic 1” or “writing Logic 1 for the bit.” Similarly, “clear a bit” is synonymous with “bit is set to Logic 0” or “writing Logic 0 for the bit.”

Table 15. Memory Map Register

Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
Chip Configuration Registers											
00	chip_port_config	0	LSB first 1 = on 0 = off (default)	Soft reset 1 = on 0 = off (default)	1	1	Soft reset 1 = on 0 = off (default)	LSB first 1 = on 0 = off (default)	0	0x18	The nibbles should be mirrored so that LSB- or MSB-first mode registers correctly regardless of shift mode.
01	chip_id	8-bit Chip ID Bits 7:0 (AD9287 = 0x05), (default)								0x05	Default is unique chip ID, different for each device. This is a read-only register.
02	chip_grade	X	Child ID 6:4 (identify device variants of Chip ID) 011 = 100 MSPS			X	X	X	X	Read only	Child ID used to differentiate graded devices.
Device Index and Transfer Registers											
05	device_index_A	X	X	Clock Channel DCO 1 = on 0 = off (default)	Clock Channel FCO 1 = on 0 = off (default)	Data Channel D 1 = on (default) 0 = off	Data Channel C 1 = on (default) 0 = off	Data Channel B 1 = on (default) 0 = off	Data Channel A 1 = on (default) 0 = off	0x0F	Bits are set to determine which on-chip device receives the next write command.
FF	device_update	X	X	X	X	X	X	X	SW transfer 1 = on 0 = off (default)	0x00	Synchronously transfers data from the master shift register to the slave.
ADC Functions											
08	modes	X	X	X	X	X	Internal power-down mode 000 = chip run (default) 001 = full power-down 010 = standby 011 = reset			0x00	Determines various generic modes of chip operation.
09	clock	X	X	X	X	X	X	X	Duty cycle stabilizer 1 = on (default) 0 = off	0x01	Turns the internal duty cycle stabilizer on and off.
0D	test_io	User test mode 00 = off (default) 01 = on, single alternate 10 = on, single once 11 = on, alternate once		Reset PN long gen 1 = on 0 = off (default)	Reset PN short gen 1 = on 0 = off (default)	Output test mode—see Table 9 in the Digital Outputs and Timing section 0000 = off (default) 0001 = midscale short 0010 = +FS short 0011 = −FS short 0100 = checker board output 0101 = PN 23 sequence 0110 = PN 9 0111 = one/zero word toggle 1000 = user input 1001 = one/zero bit toggle 1010 = 1× sync 1011 = one bit high 1100 = mixed bit frequency (format determined by output_mode)				0x00	When set, the test data is placed on the output pins in place of normal data.

Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
14	output_mode	X	0 = LVDS ANSI (default) 1 = LVDS low power, (IEEE 1596.3 similar)	X	X	X	Output invert 1 = on 0 = off (default)	00 = offset binary (default) 01 = twos complement		0x00	Configures the outputs and the format of the data.
15	output_adjust	X	X	Output driver termination 00 = none (default) 01 = 200 Ω 10 = 100 Ω 11 = 100 Ω		X	X	X	X	0x00	Determines LVDS or other output properties. Primarily functions to set the LVDS span and common-mode levels in place of an external resistor.
16	output_phase	X	X	X	X	0011 = output clock phase adjust (0000 through 1010) (Default: 180° relative to DATA edge) 0000 = 0° relative to DATA edge 0001 = 60° relative to DATA edge 0010 = 120° relative to DATA edge 0011 = 180° relative to DATA edge 0100 = 240° relative to DATA edge 0101 = 300° relative to DATA edge 0110 = 360° relative to DATA edge 0111 = 420° relative to DATA edge 1000 = 480° relative to DATA edge 1001 = 540° relative to DATA edge 1010 = 600° relative to DATA edge 1011 to 1111 = 660° relative to DATA edge				0x03	On devices that utilize global clock divide, determines which phase of the divider output is used to supply the output clock. Internal latching is unaffected.
19	user_patt1_lsb	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-defined pattern, 1 LSB.
1A	user_patt1_msb	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-defined pattern, 1 MSB.
1B	user_patt2_lsb	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-defined pattern, 2 LSB.
1C	user_patt2_msb	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-defined pattern, 2 MSB.
21	serial_control	LSB first 1 = on 0 = off (default)	X	X	X	<10 MSPS, low encode rate mode 1 = on 0 = off (default)	000 = 8 bits (default, normal bit stream) 001 = 8 bits 010 = 10 bits 011 = 12 bits 100 = 14 bits			0x00	Serial stream control. Default causes MSB first and the native bit stream (global).
22	serial_ch_stat	X	X	X	X	X	X	Channel output reset 1 = on 0 = off (default)	Channel power-down 1 = on 0 = off (default)	0x00	Used to power down individual sections of a converter (local).

Power and Ground Recommendations

When connecting power to the AD9287, it is recommended that two separate 1.8 V supplies be used: one for analog (AVDD) and one for digital (DRVDD). If only one supply is available, it should be routed to the AVDD first and then tapped off and isolated with a ferrite bead or a filter choke preceded by decoupling capacitors for the DRVDD. The user can employ several different decoupling capacitors to cover both high and low frequencies. These should be located close to the point of entry at the PC board level and close to the parts with minimal trace length.

A single PC board ground plane should be sufficient when using the AD9287. With proper decoupling and smart partitioning of the PC board's analog, digital, and clock sections, optimum performance is easily achieved.

Exposed Paddle Thermal Heat Slug Recommendations

It is required that the exposed paddle on the underside of the ADC is connected to analog ground (AGND) to achieve the best electrical and thermal performance of the AD9287. An exposed continuous copper plane on the PCB should mate to the AD9287 exposed paddle, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be solder filled or plugged.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous copper plane by overlaying a silkscreen on the PCB into several uniform sections. This provides several tie points between the two during the reflow process. Using one continuous plane with no partitions only guarantees one tie point between the ADC and PCB. See Figure 60 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see the AN-772 Application Note, "A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)," at www.analog.com.

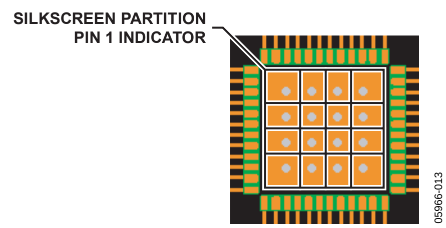


Figure 60. Typical PCB Layout

EVALUATION BOARD

The AD9287 evaluation board provides all of the support circuitry required to operate the ADC in its various modes and configurations. The converter can be driven differentially through a transformer (default) or through the AD8332 driver. The ADC can also be driven in a single-ended fashion. Separate power pins are provided to isolate the DUT from the AD8332 drive circuitry. Each input configuration can be selected by proper connection of various jumpers (see Figure 63 to Figure 67). Figure 61 shows the typical bench characterization setup used to evaluate the ac performance of the AD9287. It is critical that the signal sources used for the analog input and clock have very low phase noise (<1 ps rms jitter) to realize the optimum performance of the converter. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is also necessary to achieve the specified noise performance.

See Figure 63 to Figure 71 for the complete schematics and layout diagrams that demonstrate the routing and grounding techniques that should be applied at the system level.

POWER SUPPLIES

This evaluation board comes with a wall-mountable switching power supply that provides a 6 V, 2 A maximum output. Simply connect the supply to the rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz. The other end is a 2.1 mm inner diameter jack that connects to the PCB at P503. Once on the PC board, the 6 V supply is fused and conditioned before connecting to three low dropout linear regulators that supply the proper bias to each of the various sections on the board.

When operating the evaluation board in a nondefault condition, L504 to L507 can be removed to disconnect the switching power supply. This enables the user to bias each section of the board individually. Use P501 to connect a different supply for each section. At least one 1.8 V supply is needed with a 1 A current capability for AVDD_DUT and DRVDD_DUT; however, it is recommended that separate supplies be used for both analog and digital. To operate the evaluation board using the VGA option, a separate 5.0 V analog supply is needed. The 5.0 V supply, or AVDD_5 V, should have a 1 A current capability. To operate the evaluation board using the SPI and alternate clock options, a separate 3.3 V analog supply is needed in addition to the other supplies. The 3.3 V supply, or AVDD_3.3 V, should have a 1 A current capability as well.

INPUT SIGNALS

When connecting the clock and analog source, use clean signal generators with low phase noise, such as Rohde & Schwarz SMHU or HP8644 signal generators or the equivalent. Use a 1 m, shielded, RG-58, 50 Ω coaxial cable for making connections to the evaluation board. Enter the desired frequency and amplitude from the ADC specifications tables. Typically, most ADI evaluation boards can accept ~2.8 V p-p or 13 dBm sine wave input for the clock. When connecting the analog input source, it is recommended to use a multipole, narrow-band, band-pass filter with 50 Ω terminations. ADI uses TTE, Allen Avionics, and K&L types of band-pass filters. The filter should be connected directly to the evaluation board if possible.

OUTPUT SIGNALS

The default setup uses the HSC-ADC-FPGA high speed deserialization board to deserialize the digital output data and convert it to parallel CMOS. These two channels interface directly with the ADI standard dual-channel FIFO data capture board (HSC-ADC-EVALA-DC). Two of the four channels can then be evaluated at the same time. For more information on channel settings on these boards and their optional settings, visit www.analog.com/FIFO.

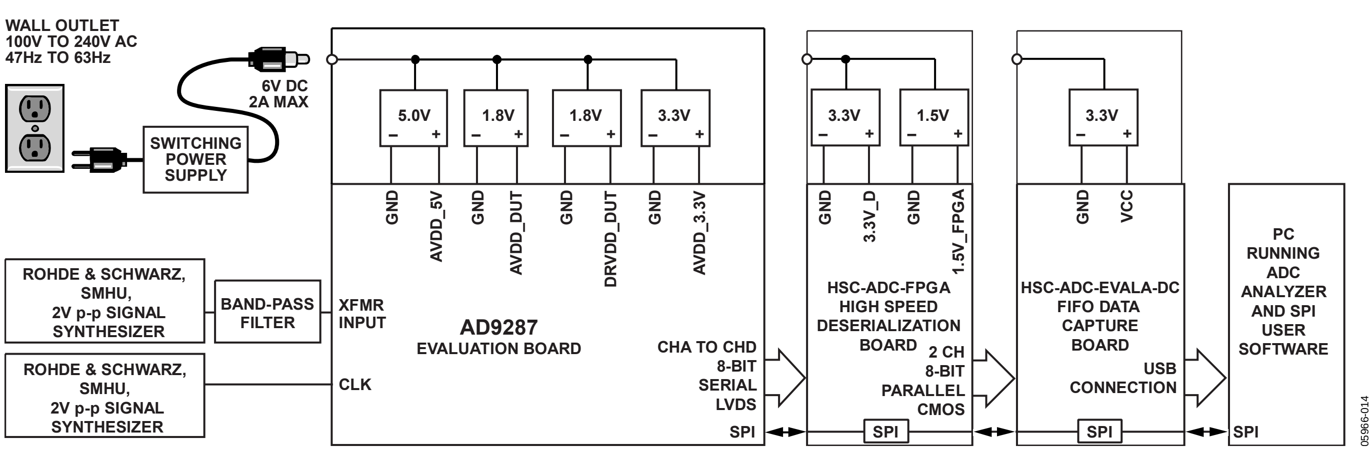


Figure 61. Evaluation Board Connection

DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

The following is a list of the default and optional settings or modes allowed on the AD9287 Rev. A evaluation board.

- POWER: Connect the switching power supply that is supplied in the evaluation kit between a rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz and P503.
- AIN: The evaluation board is set up for a transformer-coupled analog input with optimum 50 Ω impedance matching out to 190 MHz (see Figure 62). For more bandwidth response, the differential capacitor across the analog inputs can be changed or removed. The common mode of the analog inputs is developed from the center tap of the transformer or AVDD_DUT/2.

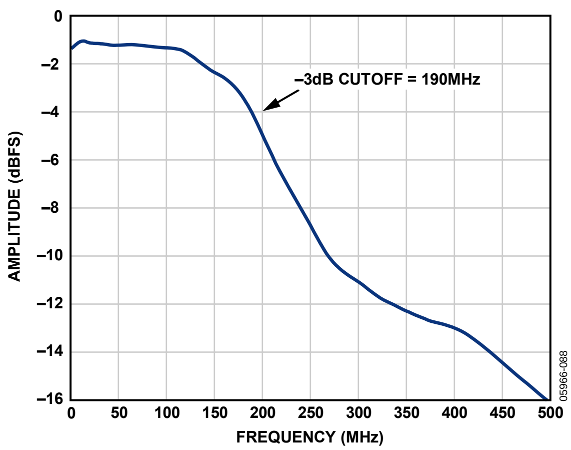


Figure 62. Evaluation Board Full Power Bandwidth

- VREF: VREF is set to 1.0 V by tying the SENSE pin to ground, R237. This causes the ADC to operate in 2.0 V p-p full-scale range. A separate external reference option using the ADR510 or ADR520 is also included on the evaluation board. Simply populate R231 and R235 and remove C214. Proper use of the VREF options is noted in the Voltage Reference section.
- RBIAS: RBIAS has a default setting of 10 kΩ (R201) to ground and is used to set the ADC core bias current. To further lower the core power (excluding the LVDS driver supply), simply change the resistor setting. However, performance of the ADC will degrade depending on the resistor chosen. See RBIAS section for more information.
- CLOCK: The default clock input circuitry is derived from a simple transformer-coupled circuit using a high bandwidth 1:1 impedance ratio transformer (T201) that adds a very low amount of jitter to the clock path. The clock input is 50 Ω terminated and ac-coupled to handle single-ended sine wave types of inputs. The transformer converts the single-ended input to a differential signal that is clipped before entering the ADC clock inputs.

  A differential LVPECL clock can also be used to clock the ADC input using the AD9515 (U202). Simply populate R225 and R227 with 0 Ω resistors and remove R217 and R218 to disconnect the default clock path inputs. In addition, populate C207 and C208 with a 0.1 μF capacitor and remove C210 and C211 to disconnect the default cloth path outputs. The AD9515 has many pin-strappable options that are set to a default working condition. Consult the AD9515 data sheet for more information about these and other options.

  If using an oscillator, two oscillator footprint options are also available (OSC201) to check the ADC performance. J205 gives the user flexibility in using the enable pin, which is common on most oscillators.

- PDWN: To enable the power-down feature, simply short J201 to the on position (AVDD) on the PDWN pin.
- SCLK/DTP: To enable the digital test patterns on the digital outputs of the ADC, use J204. If J204 is tied to AVDD during device power-up, Test Pattern 1000 0000 will be enabled. See the SCLK/DTP Pin section for details.
- SDIO/ODM: To enable the low power, reduced signal option similar to the IEEE 1595.3 reduced range link LVDS output standard, use J203. If J203 is tied to AVDD during device power-up, it enables the LVDS outputs in a low power, reduced signal option from the default ANSI standard. This option changes the signal swing from 350 mV p-p to 200 mV p-p, which reduces the power of the DRVDD supply. See the SDIO/ODM Pin section for more details.
- CSB: To enable the SPI information on the SDIO and SCLK pins that is to be processed, simply tie J202 low in the always enable mode. To ignore the SDIO and SCLK information, tie J202 to AVDD.
- Non-SPI Mode: For users who wish to operate the DUT without using SPI, simply remove Jumpers J202, J203, and J204. This disconnects the CSB, SCLK/DTP, and SDIO/OMD pins from the control bus, allowing the DUT to operate in its simplest mode. Each of these pins has internal termination and will float to its respective level.
- D+, D−: If an alternative data capture method to the setup described in Figure 61 is used, optional receiver terminations, R206 to R211, can be installed next to the high speed back-plane connector.

ALTERNATIVE ANALOG INPUT DRIVE CONFIGURATION

The following is a brief description of the alternative analog input drive configuration using the AD8332 dual VGA. If this particular drive option is in use, some components may need to be populated, in which case all the necessary components are listed in Table 16. For more details on the AD8332 dual VGA, including how it works and its optional pin settings, consult the AD8332 data sheet.

To configure the analog input to drive the VGA instead of the default transformer option, the following components need to be removed and/or changed.

- Remove R102, R115, R128, R141, T101, T102, T103, and T104 in the default analog input path.
- Populate R101, R114, R127, and R140 with 0 Ω resistors in the analog input path.
- Populate R106, R107, R119, R120, R132, R133, R144, and R145 with 10 kΩ resistors to provide an input common-mode level to the analog input.
- Populate R105, R113, R118, R124, R131, R137, R151, and R160 with 0 Ω resistors in the analog input path.

Currently, L301 to L308 and L401 to L408 are populated with 0 Ω resistors to allow signal connection. This area allows the user to design a filter if additional requirements are necessary.

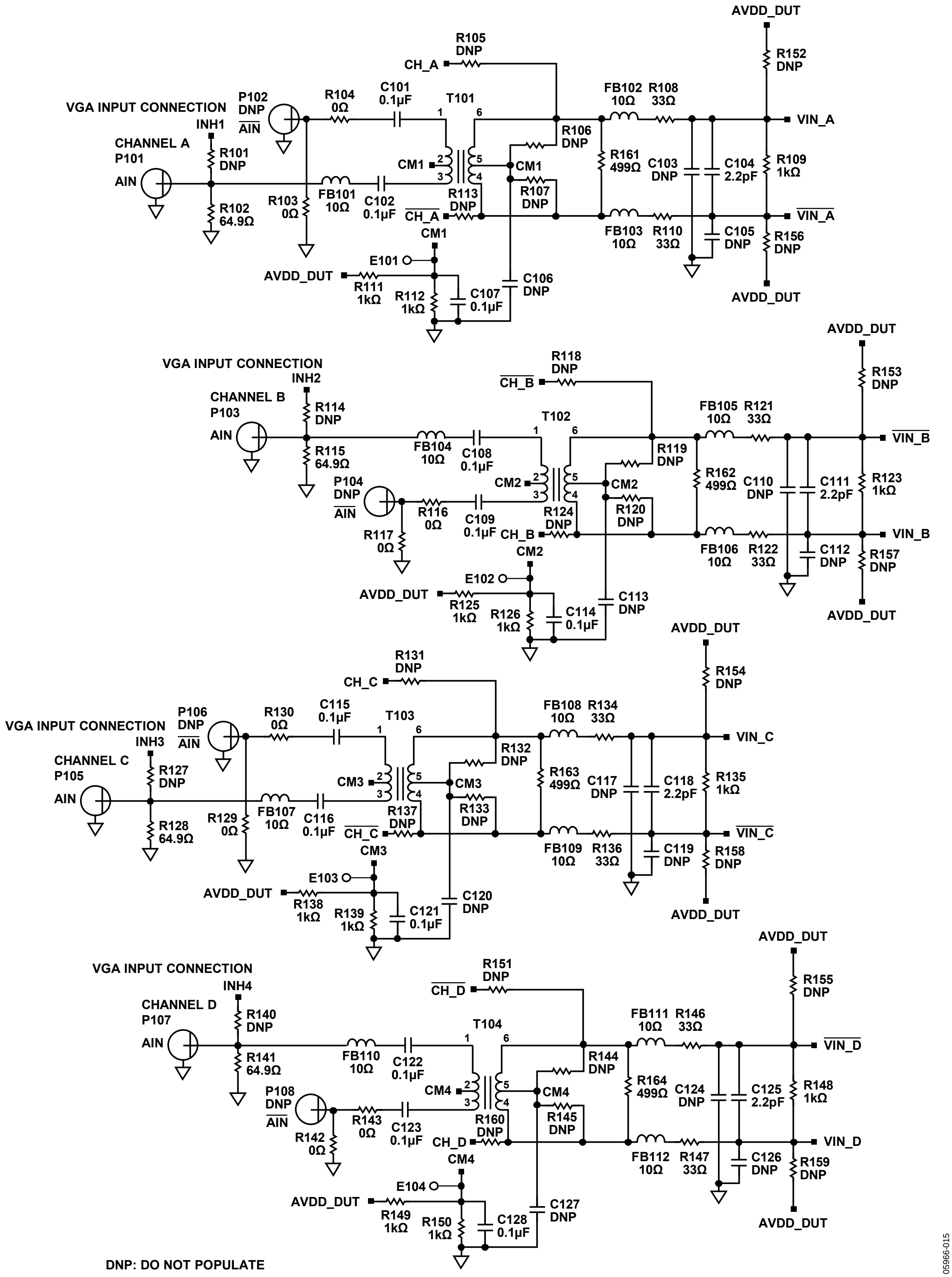


Figure 63. Evaluation Board Schematic, DUT Analog Inputs

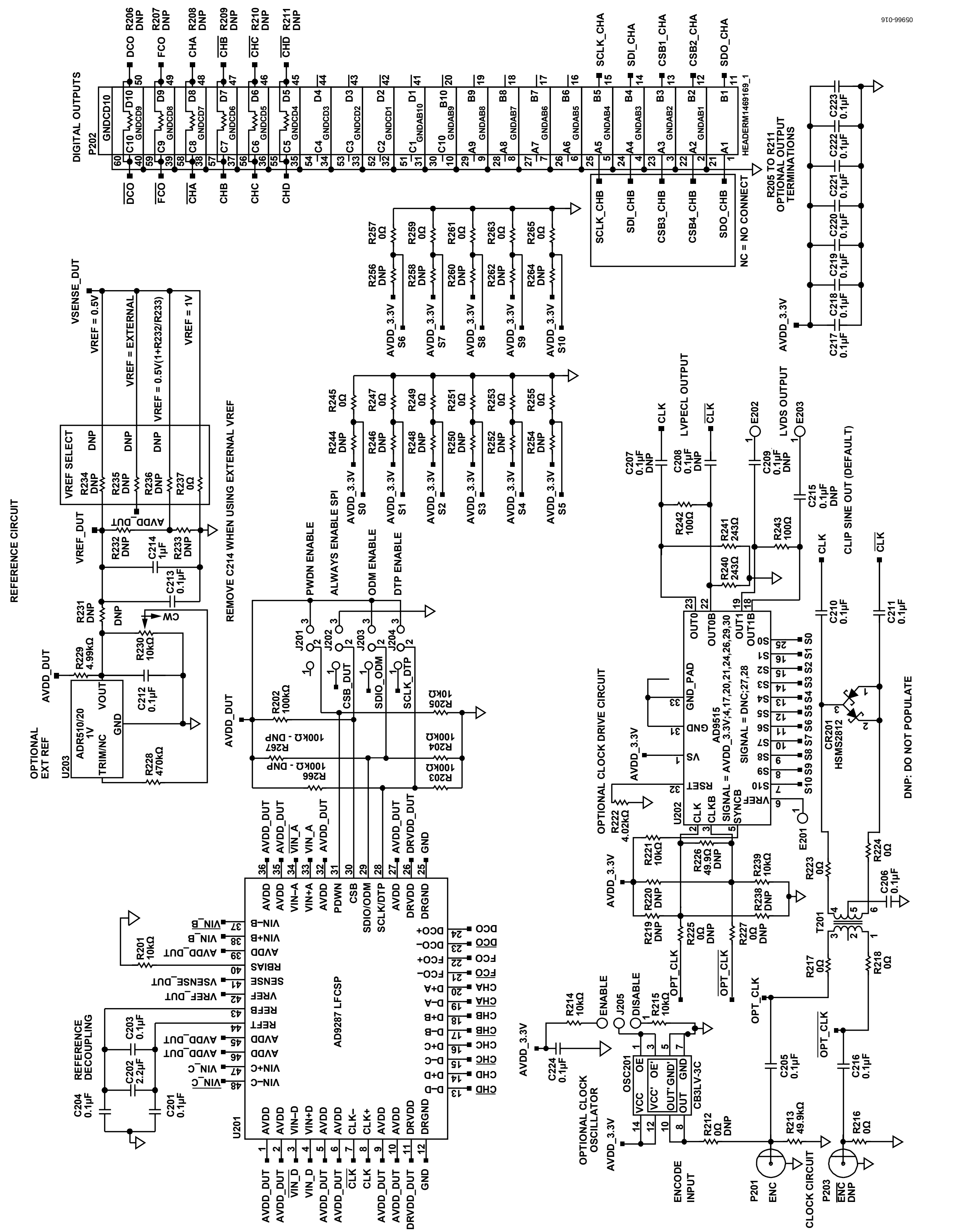


Figure 64. Evaluation Board Schematic, DUT, VREF, Clock Inputs, and Digital Output Interface

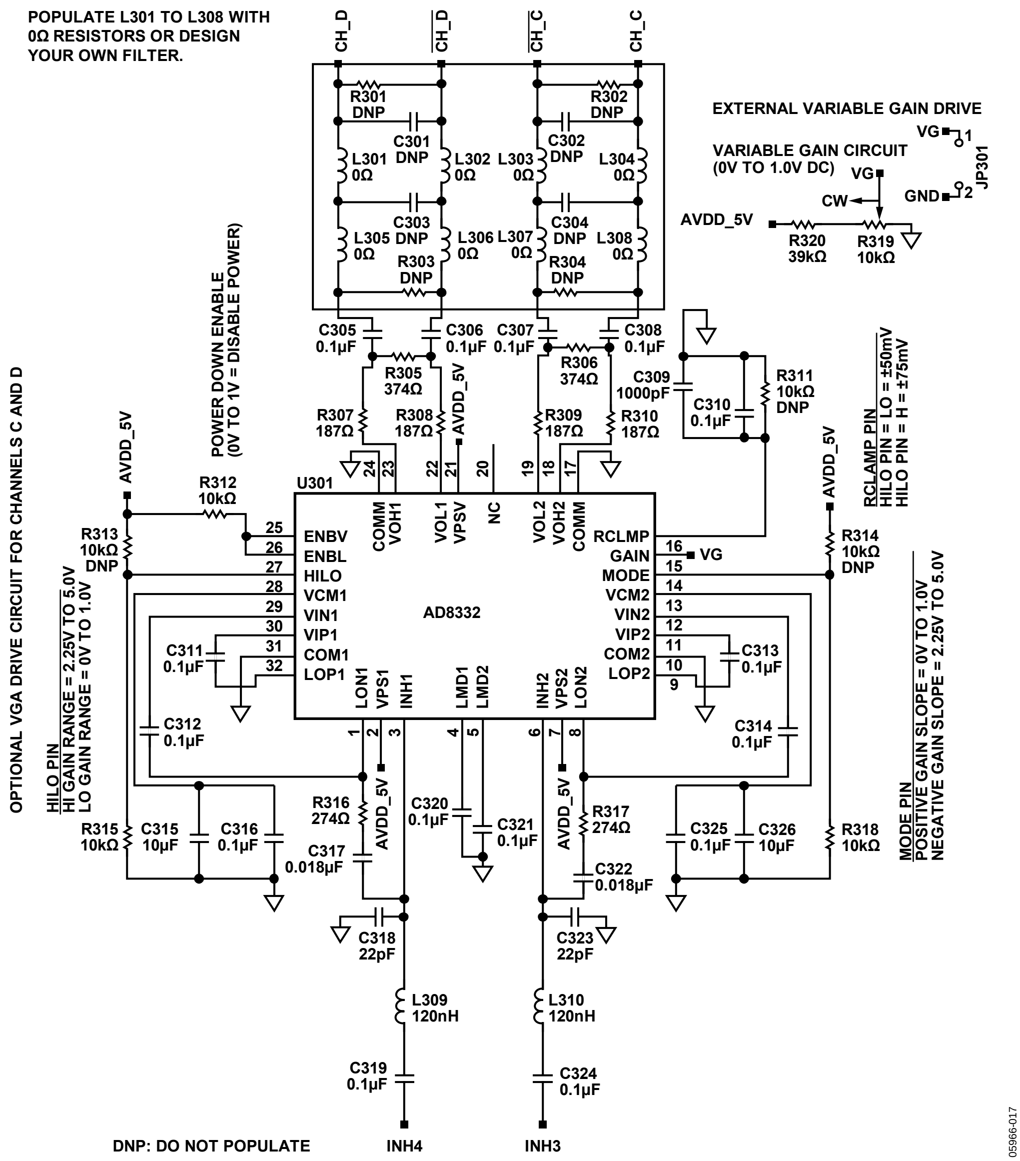


Figure 65. Evaluation Board Schematic, Optional DUT Analog Input Drive

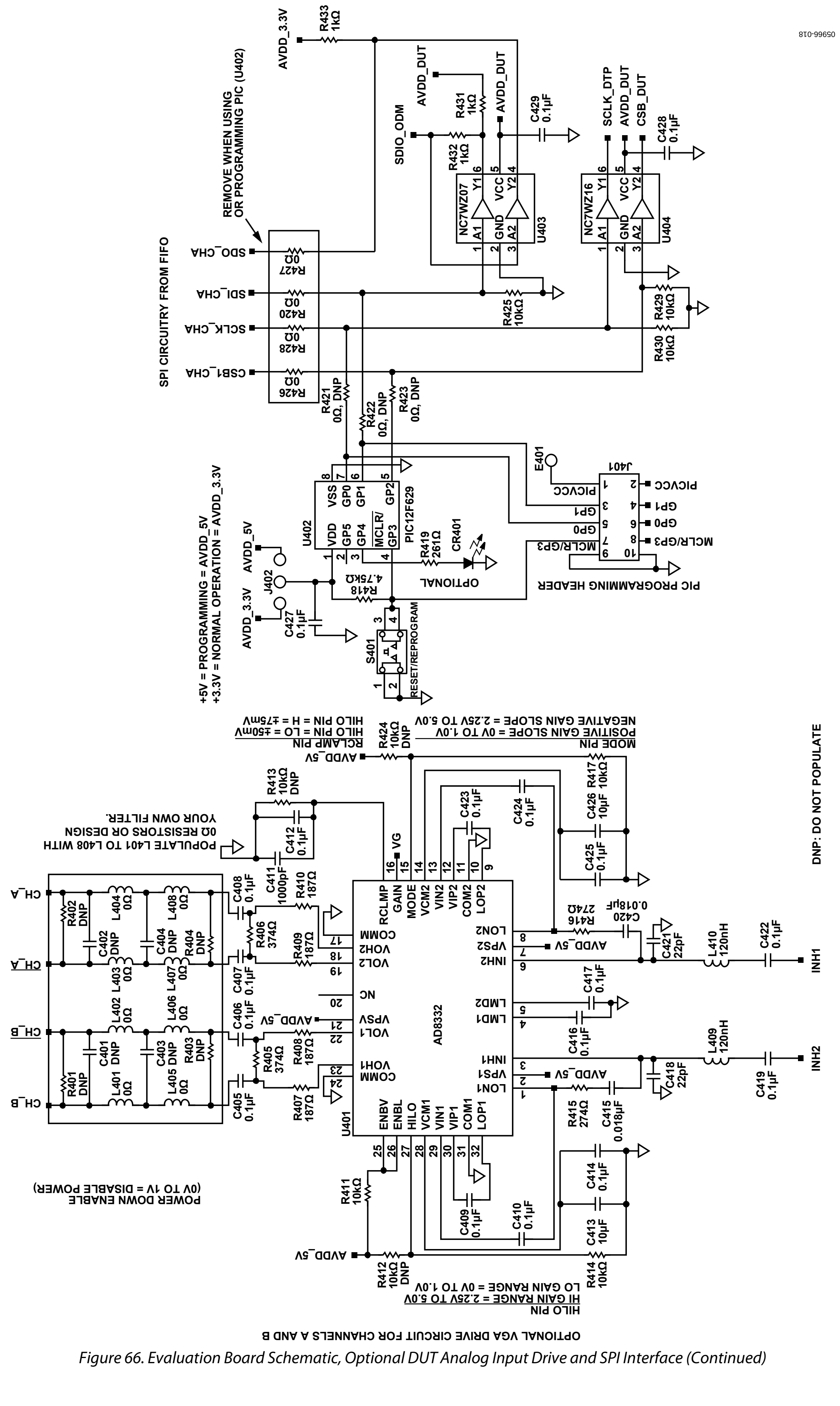


Figure 66. Evaluation Board Schematic, Optional DUT Analog Input Drive and SPI Interface (Continued)

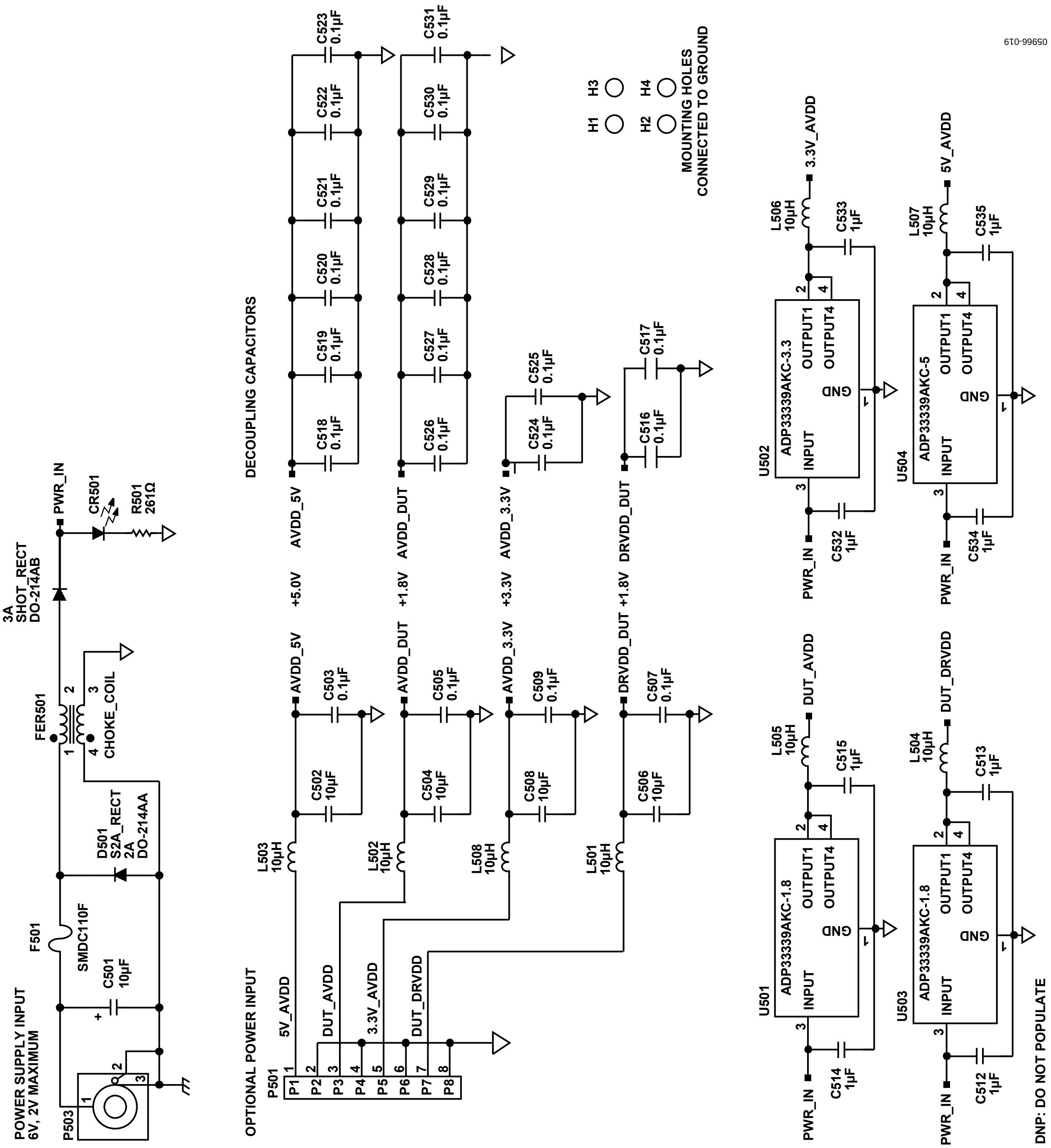
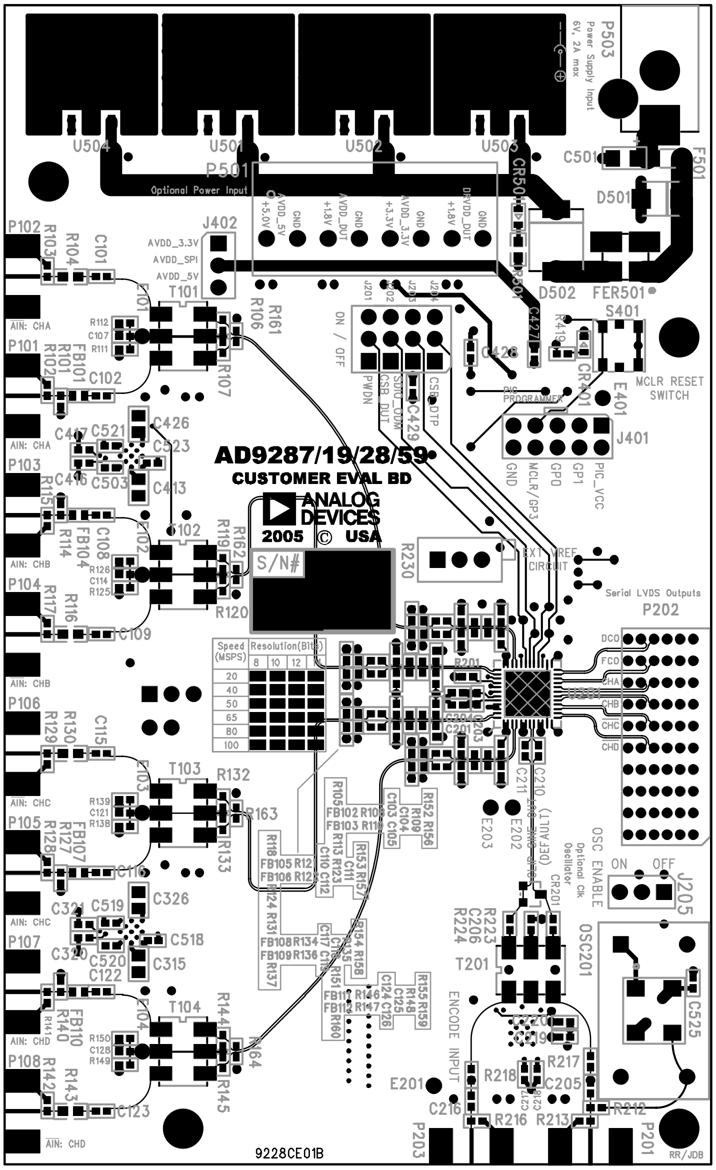


Figure 67. Evaluation Board Schematic, Power Supply Inputs



05966-020

Figure 68. Evaluation Board Layout, Primary Side

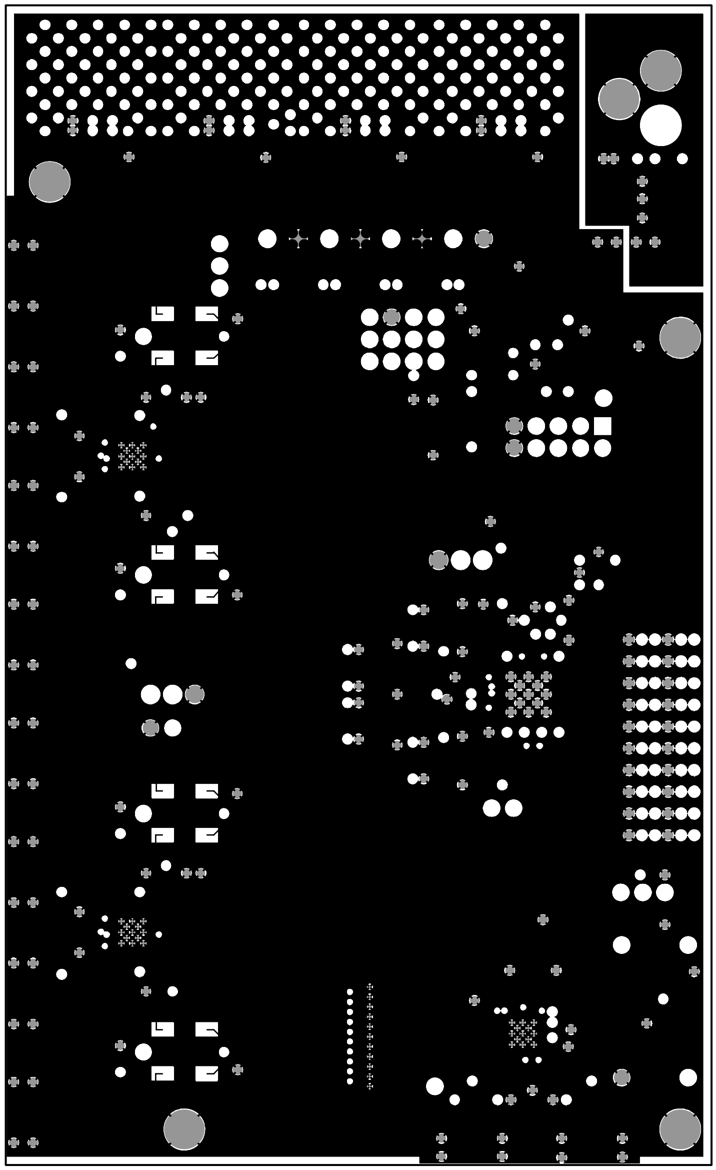


Figure 69. Evaluation Board Layout, Ground Plane

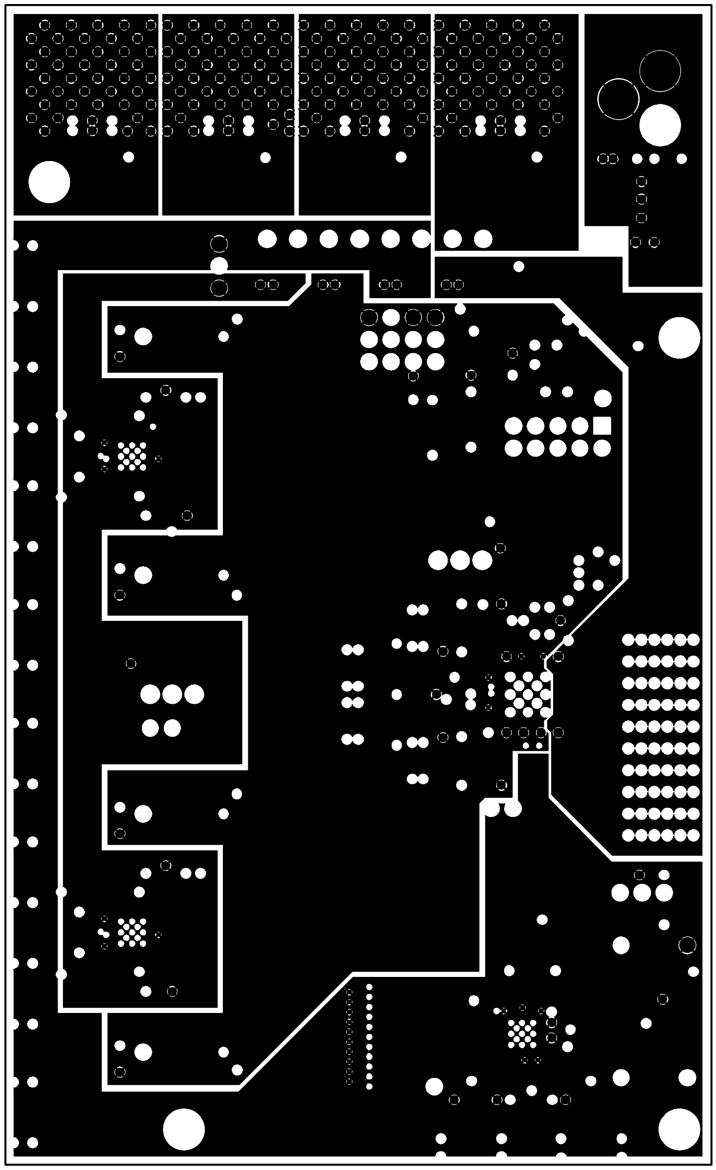


Figure 70. Evaluation Board Layout, Power Plane

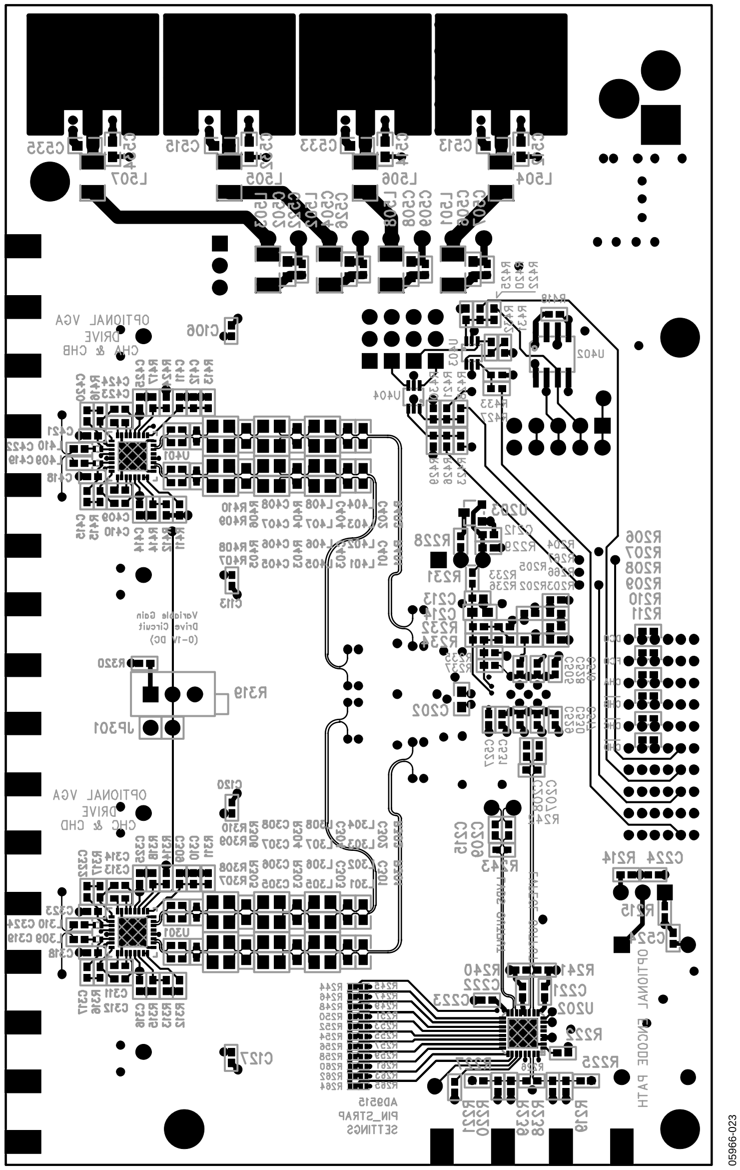


Figure 71. Evaluation Board Layout, Secondary Side (Mirrored Image)

Table 16. Evaluation Board Bill of Materials (BOM)

Item	Qnty. per Board	REFDES	Device	Pkg.	Value	Mfg.	Mfg. Part Number
1	1	AD9287LFCSP_REVA	PCB	PCB	PCB		
2	75	C101, C102, C107, C108, C109, C114, C115, C116, C121, C122, C123, C128, C201, C203, C204, C205, C206, C210, C211, C212, C213, C216, C217, C218, C219, C220, C221, C222, C223, C224, C310, C311, C312, C313, C314, C316, C319, C320, C321, C324, C325, C409, C410, C412, C414, C416, C417, C419, C422, C423, C424, C425, C427, C428, C429, C503, C505, C507, C509, C516, C517, C518, C519, C520, C521, C522, C523, C524, C525, C526, C527, C528, C529, C530, C531	Capacitor	402	0.1 µF, ceramic, X5R, 10 V, 10% tol	Panasonic	ECJ-0EB1A104K
3	4	C104, C111, C118, C125	Capacitor	402	2.2 pF, ceramic, COG, 0.25 pF tol, 50 V	Murata	GRM1555C1H2R2GZ01B
4	4	C315, C326, C413, C426	Capacitor	805	10 µF, 6.3 V ±10% ceramic, X5R	AVX	08056D106KAT2A
5	1	C202	Capacitor	603	2.2 µF, ceramic, X5R, 6.3 V, 10% tol	Panasonic	ECJ-1VB0J225K
6	2	C309, C411	Capacitor	402	1000 pF, ceramic, X7R, 25 V, 10% tol	Kemet	C0402C102K3RACTU
7	4	C317, C322, C415, C420	Capacitor	402	0.018 µF, ceramic, X7R, 16 V, 10% tol	AVX	0402YC183KAT2A
8	4	C318, C323, C418, C421	Capacitor	402	22 pF, ceramic, NPO, 5% tol, 50 V	Kemet	C0402C220J5GACTU
9	1	C501	Capacitor	1206	10 µF, tantalum, 16 V, 20% tol	Rohm	TCA1C106M8R
10	9	C214, C512, C513, C514, C515, C532, C533, C534, C535	Capacitor	603	1 µF, ceramic, X5R, 6.3 V, 10% tol	Panasonic	ECJ-1VB0J105K
11	8	C305, C306, C307, C308, C405, C406, C407, C408	Capacitor	805	0.1 µF, ceramic, X7R, 50 V, 10% tol	AVX	08055C104KAT2A
12	4	C502, C504, C506, C508	Capacitor	603	10 µF, ceramic, X5R, 6.3 V, 20% tol	Panasonic	ECJ-1VB0J106M
13	1	CR201	Diode	SOT-23	30 V, 20 mA, dual Schottky	Agilent Technologies	HSMS2812
14	2	CR401, CR501	LED	603	Green, 4 V, 5 m candela	Panasonic	LNJ306G8TRA
15	1	D502	Diode	DO-214AB	3 A, 30 V, SMC	Micro Commercial Co.	SK33MSCT
16	1	D501	Diode	DO-214AA	2 A, 50 V, SMC	Micro Commercial Co.	S2A

Item	Qnty. per Board	REFDES	Device	Pkg.	Value	Mfg.	Mfg. Part Number
17	1	F501	Fuse	1210	6.0 V, 2.2 A trip-current resettable fuse	Tyco/Raychem	NANOSMDC110F-2
18	1	FER501	Choke Coil	2020	10 µH, 5 A, 50 V, 190 Ω @ 100 MHz	Murata	DLW5BSN191SQ2L
19	12	FB101, FB102, FB103, FB104, FB105, FB106, FB107, FB108, FB109, FB110, FB111, FB112	Ferrite bead	603	10 Ω, test freq 100 MHz, 25% tol, 500 mA	Murata	BLM18BA100SN1
20	1	JP301	Connector	2-pin	100 mil header jumper, 2-pin	Samtec	TSW-102-07-G-S
21	2	J205, J402	Connector	3-pin	100 mil header jumper, 3-pin	Samtec	TSW-103-07-G-S
22	1	J201 to J204	Connector	12-pin	100 mil header male, 4 × 3 triple row straight	Samtec	TSW-104-08-G-T
23	1	J401	Connector	10-pin	100 mil header, male, 2 × 5 double row straight	Samtec	TSW-105-08-G-D
24	8	L501, L502, L503, L504, L505, L506, L507, L508	Ferrite bead	1210	10 µH, bead core 3.2 × 2.5 × 1.6 SMD, 2 A	Panasonic-ECG	EXC-CL3225U1
25	4	L309, L310, L409, L410	Inductor	402	120 nH, test freq 100 MHz, 5% tol, 150 mA	Murata	LQG15HNR12J02B
26	16	L301, L302, L303, L304, L305, L306, L307, L308, L401, L402, L403, L404, L405, L406, L407, L408	Resistor	805	0 Ω, 1/8 W, 5% tol	Panasonic	ERJ-6GEY0R00V
27	1	OSC201	Oscillator	SMT	Clock oscillator, 100.00 MHz, 3.3 V	CTS REEVES	CB3LV-3C-100M0000-T
28	5	P101, P103, P105, P107, P201	Connector	SMA	Side-mount SMA for 0.063" board thickness	Johnson Components	142-0711-821
29	1	P202	Connector	HEADER	1469169-1, right angle 2-pair, 25 mm, header assembly	Tyco	1469169-1
30	1	P503	Connector	0.1", PCMT	RAPC722, power supply connector	Switchcraft	SC1153
31	15	R201, R205, R214, R215, R221, R239, R312, R315, R318, R411, R414, R417, R425, R429, R430	Resistor	402	10 kΩ, 1/16 W, 5% tol	Panasonic	ERJ-2GEJ103X
32	14	R103, R117, R129, R142, R216, R217, R218, R223, R224, R237, R420, R426, R427, R428	Resistor	402	0 Ω, 1/16 W, 5% tol	Panasonic	ERJ-2GE0R00X
33	4	R102, R115, R128, R141	Resistor	402	64.9 Ω, 1/16 W, 1% tol	Panasonic	ERJ-2RKF64R9X
34	4	R104, R116, R130, R143	Resistor	603	0 Ω, 1/10 W, 5% tol	Panasonic	ERJ-3GEY0R00V

Item	Qnty. per Board	REFDES	Device	Pkg.	Value	Mfg.	Mfg. Part Number
35	15	R109, R111, R112, R123, R125, R126, R135, R138, R139, R148, R149, R150, R431, R432, R433	Resistor	402	1 kΩ, 1/16 W, 1% tol	Panasonic	ERJ-2RKF1001X
36	8	R108, R110, R121, R122, R134, R136, R146, R147	Resistor	402	33 Ω, 1/16 W, 5% tol	Panasonic	ERJ-2GEJ330X
37	4	R161, R162, R163, R164	Resistor	402	499 Ω, 1/16 W, 1% tol	Panasonic	ERJ-2RKF4990X
38	3	R202, R203, R204	Resistor	402	100 kΩ, 1/16 W, 1% tol	Panasonic	ERJ-2RKF1003X
39	1	R222	Resistor	402	4.02 kΩ, 1/16 W, 1% tol	Panasonic	ERJ-2RKF4021X
40	1	R213	Resistor	402	49.9 Ω, 1/16 W, 0.5% tol	Susumu	RR0510R-49R9-D
41	1	R229	Resistor	402	4.99 kΩ, 1/16 W, 5% tol	Panasonic	ERJ-2RKF4991X
42	2	R230, R319	Potentiometer	3-lead	10 kΩ, Cermet trimmer potentiometer, 18 turn top adjust, 10%, 1/2 W	BC Components	CT-94W-103
43	1	R228	Resistor	402	470 kΩ, 1/16 W, 5% tol	Yageo America	9C04021A4703JLHF3
44	1	R320	Resistor	402	39 kΩ, 1/16 W, 5% tol	Susumu	RR0510P-393-D
45	8	R307, R308, R309, R310, R407, R408, R409, R410	Resistor	402	187 Ω, 1/16 W, 1% tol	Panasonic	ERJ-2RKF1870X
46	4	R305, R306, R405, R406	Resistor	402	374 Ω, 1/16 W, 1% tol	Panasonic	ERJ-2RKF3740X
47	4	R316, R317, R415, R416	Resistor	402	274 Ω, 1/16 W, 1% tol	Panasonic	ERJ-2RKF2740X
48	11	R245, R247, R249, R251, R253, R255, R257, R259, R261, R263, R265	Resistor	201	0 Ω, 1/20 W, 5% tol	Panasonic	ERJ-1GE0R00C
49	1	R418	Resistor	402	4.75 kΩ, 1/16 W, 1% tol	Panasonic	ERJ-2RKF4751X
50	1	R419	Resistor	402	261 Ω, 1/16 W, 1% tol	Panasonic	ERJ-2RKF2610X
51	1	R501	Resistor	603	261 Ω, 1/16 W, 1% tol	Panasonic	ERJ-3EKF2610V
52	2	R240, R241	Resistor	402	243 Ω, 1/16 W, 1% tol	Panasonic	ERJ-2RKF2430X
53	2	R242, R243	Resistor	402	100 Ω, 1/16 W, 1% tol	Panasonic	ERJ-2RKF1000X
54	1	S401	Switch	SMD	LIGHT TOUCH, 100GE, 5 mm	Panasonic	EVQ-PLDA15
55	5	T101, T102, T103, T104, T201	Transformer	CD542	ADT1-1WT, 1:1 impedance ratio transformer	Mini-Circuits	ADT1-1WT
56	2	U501, U503	IC	SOT-223	ADP33339AKC-1.8, 1.5 A, 1.8 V LDO regulator	ADI	ADP33339AKC-1.8

Item	Qnty. per Board	REFDES	Device	Pkg.	Value	Mfg.	Mfg. Part Number
57	2	U301, U401	IC	LFCSP, CP-32	AD8332ACP, ultralow noise precision dual VGA	ADI	AD8332ACP
58	1	U504	IC	SOT-223	ADP33339AKC-5	ADI	ADP33339AKC-5
59	1	U502	IC	SOT-223	ADP33339AKC-3.3	ADI	ADP33339AKC-3.3
60	1	U201	IC	LFCSP, CP-48-1	AD9287-100, quad, 8-bit, 100 MSPS serial LVDS 1.8 V ADC	ADI	AD9287BCPZ-100
61	1	U203	IC	SOT-23	ADR510AR, 1.0 V, precision low noise shunt voltage reference	ADI	ADR510AR
62	1	U202	IC	LFCSP CP-32-2	AD9515	ADI	AD9515BCPZ
63	1	U403	IC	SC70, MAA06A	NC7WZ07	Fairchild	NC7WZ07P6X
64	1	U404	IC	SC70, MAA06A	NC7WZ16	Fairchild	NC7WZ16P6X
65	1	U402	IC	8-SOIC	Flash prog mem 1kx14, RAM size 64 × 8, 20 MHz speed, PIC12F controller series	Microchip	PIC12F629-I/SN

OUTLINE DIMENSIONS

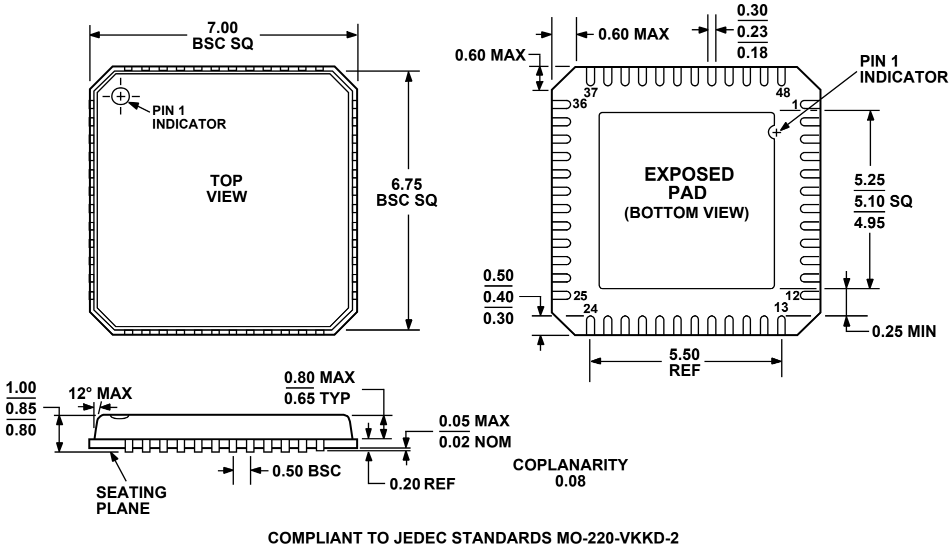


*Figure 72. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad
(CP-48-1)
Dimensions shown in millimeters*

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9287BCPZ-100[1]	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-1
AD9287BCPZRL-100[1]	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ] Tape and Reel	CP-48-1
AD9287-100EB		Evaluation Board	

[1] Z = Pb-free part.

NOTES

NOTES

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